# EFR32FG25 Gecko Wireless SoC Family Data Sheet

The EFR32FG25 Gecko SoC is an ideal solution for sub-GHz Wi-SUN applications for metering, lighting, and distribution automation.

The high-performance sub-GHz radio provides long range and is resistant to interference from 2.4 GHz technologies such as Wi-Fi.

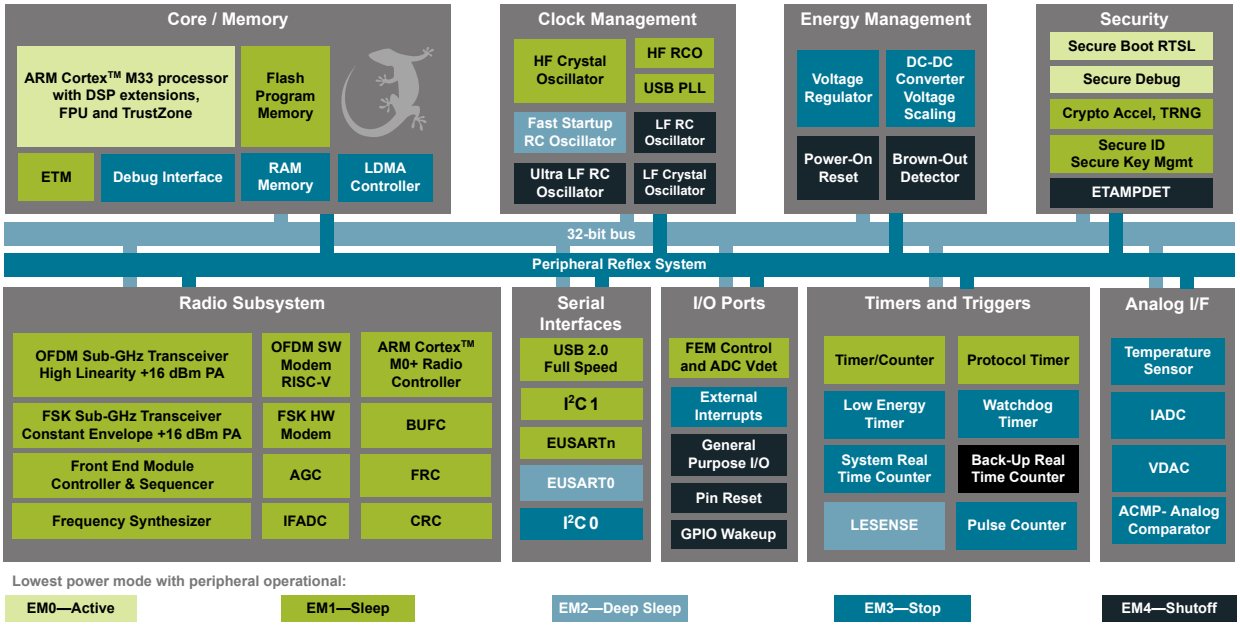
The single-die, multi-core solution provides industry leading security, high throughput, and an integrated power amplifier for secure IoT devices connectivity.

EFR32FG25 applications include:

- Smart electric metering
- Street lighting
- Distribution automation
- Industrial applications
- Municipal infrastructure

**KEY FEATURES**

- 32-bit ARM® Cortex®-M33 core with 97.5 MHz maximum operating frequency
- Up to 1920 KB of flash and 512 KB of RAM
- Wi-SUN Multi-rate OFDM, FSK, and O-QPSK modulations
- Integrated PA with up to 16 dBm (sub-GHz) TX power
- Robust peripheral set and up to 37 GPIO
- Operating temperature up to 125 °C



# 1. Feature List

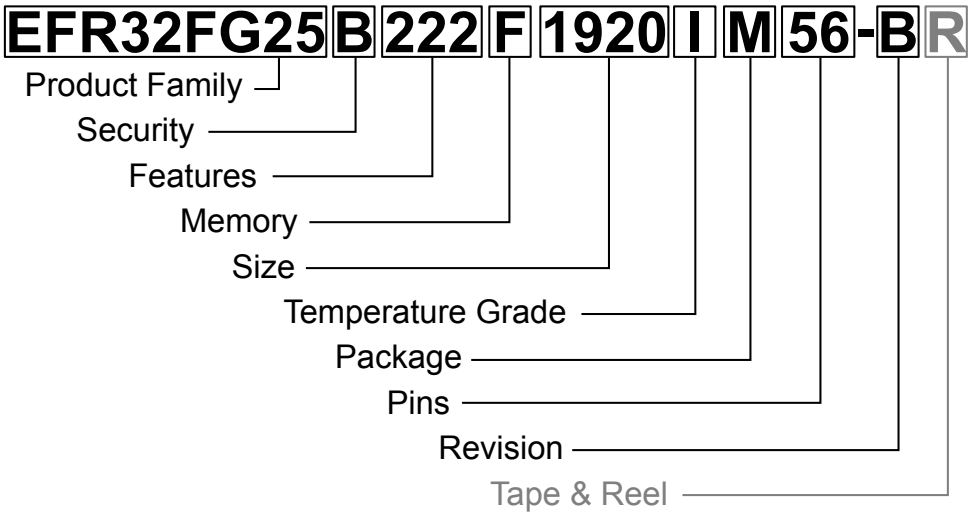
The EFR32FG25 highlighted features are listed below.

- **Low-power Wireless System-on-Chip**
  - High-performance 32-bit 97.5 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 1920 KB flash program memory
  - Up to 512 KB RAM data memory
  - Sub-GHz radio operation
  - TX power up to 16 dBm
- **Low Energy Consumption**
  - 6.3 mA RX current at 924 MHz (400 kbps 4-GFSK)
  - 58.6 mA TX current @ 13 dBm output power at 923.6 MHz with CW from FSK PA
  - 76.6 mA TX current @ 16 dBm output power at 915 MHz with CW from FSK PA
  - 186 mA TX current @ 16 dBm output power at 914 MHz (2.4 Mbps Wi-SUN OFDM Option 1, MCS6)
  - 30 µA/MHz in Active Mode (EM0) at 97.5 MHz
  - 4.6 µA EM2 DeepSleep current (512 KB RAM retention and RTC running from LFXO)
  - 2.6 µA EM2 DeepSleep current (32 KB RAM retention and RTC running from LFRCO)
- **High Receiver Performance**
  - -107.5 dBm sensitivity @ 300 kbps 923.7 MHz Wi-SUN OFDM Option 3, MCS4
  - -114.5 dBm sensitivity @ 50 kbps 923.6 MHz Wi-SUN FSK #1b with FEC
  - -115.8 dBm sensitivity @ 12.5 kbps 923.6 MHz Wi-SUN OFDM Option 4, MCS0
  - -125.8 dBm sensitivity @ 4.8 kbps 915 MHz O-QPSK
  - -123.9 dBm sensitivity @ 6.25 kbps 914 MHz SUN O-QPSK
  - -114.6 dBm sensitivity @ 50 kbps 914 MHz Wi-SUN FSK #1b with FEC
  - -95.3 dBm sensitivity @ 2.4 Mbps 914 MHz Wi-SUN OFDM Option 1, MCS6
  - -116.0 dBm sensitivity @ 12.5 kbps 914 MHz Wi-SUN OFDM Option 4, MCS0
  - -114.1 dBm sensitivity @ 50 kbps 866.5 MHz Wi-SUN FSK #1a with FEC
  - -113.2 dBm sensitivity @ 50 kbps 866.5 MHz OFDM Option 4, MCS2
  - -114.5 dBm sensitivity @ 50 kbps 490 MHz OFDM Option 4, MCS2
- **Supported Modulation Format**
  - Wi-SUN MR OFDM MCS 0-6 (all 4 Options)
  - 802.15.4 SUN MR O-QPSK with DSSS
  - Wi-SUN FSK
  - 2 (G)FSK with fully configurable shaping
  - (G)MSK
- **Protocol Support**
  - Proprietary
  - Wi-SUN
- **Wide Selection of MCU Peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - 2 × Analog Comparator (ACMP)
  - Digital to Analog Converter (VDAC) with two channels
  - Low-Energy Sensor Interface (LESENSE)
  - Up to 37 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 16 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 6 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 2 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 2 × Watchdog Timer
  - 1 × USB2.0 Full Speed port, Device only
  - 5 × EUSART (Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter)
    - EUSART0 operates in EM2
    - SPI and IrDA supported by EUSART
  - 2 × $I^2C$ interface with SMBus support
  - High Frequency Crystal Oscillator clock sharing using buffered sine wave clock output
  - Die temperature sensor with ±2 °C typical accuracy across temperature range
- **Wide Operating Range**
  - 1.71 to 3.8 V VDD power supply
  - 3.45 to 3.8 V PAVDD power supply for OFDM
  - 3.0 to 3.8 V PAVDD power supply without OFDM
  - -40 to +125 °C
- **Secure Vault**
  - Hardware Cryptographic Acceleration for AES128/192/256, ChaCha20-Poly1305, SHA-1, SHA-2/256/384/512, ECDSA+ECDH(P-192, P-256, P-384, P-521), Ed25519 and Curve25519, J-PAKE, PBKDF2
  - True Random Number Generator (TRNG)
  - ARM® TrustZone®
  - Secure Boot (Root of Trust Secure Loader)
  - Secure Debug Unlock
  - DPA Countermeasures
  - Secure Key Management with PUF
  - Anti-Tamper
  - External Tamper Detection with dedicated external Active Tamper I/O pairs for use with tamper shields or protecting PCB traces
  - Secure Attestation
- **Packages**
  - **QFN56** 7 × 7 × 0.85 mm

## 2. Ordering Information

**Table 2.1. Ordering Information**

| Ordering Code | Modem Feature | Max TX Power | Flash (KB) | RAM (KB) | Secure Vault | GPIO | Package / Pinout | Temp Range |
|---|---|---|---|---|---|---|---|---|
| EFR32FG25B222F1920IM56-B | • OFDM<br>• FSK<br>• O-QPSK | 16 dBm | 1920 | 512 | High | 36 | QFN56 / Clock Out | -40 to 125 °C |
| EFR32FG25B221F1920IM56-B | • OFDM<br>• FSK<br>• O-QPSK | 16 dBm | 1920 | 512 | High | 37 | QFN56 / Standard | -40 to 125 °C |
| EFR32FG25B212F1920IM56-B | • FSK<br>• O-QPSK | 16 dBm | 1920 | 512 | High | 36 | QFN56 / Clock Out | -40 to 125 °C |
| EFR32FG25B211F1920IM56-B | • FSK<br>• O-QPSK | 16 dBm | 1920 | 512 | High | 37 | QFN56 / Standard | -40 to 125 °C |
| EFR32FG25B121F1152IM56-B | • OFDM<br>• FSK<br>• O-QPSK | 16 dBm | 1152 | 256 | High | 37 | QFN56 / Standard | -40 to 125 °C |
| EFR32FG25B111F1152IM56-B | • FSK<br>• O-QPSK | 16 dBm | 1152 | 256 | High | 37 | QFN56 / Standard | -40 to 125 °C |
| EFR32FG25A221F1920IM56-B | • OFDM<br>• FSK<br>• O-QPSK | 16 dBm | 1920 | 512 | Mid | 37 | QFN56 / Standard | -40 to 125 °C |
| EFR32FG25A211F1920IM56-B | • FSK<br>• O-QPSK | 16 dBm | 1920 | 512 | Mid | 37 | QFN56 / Standard | -40 to 125 °C |
| EFR32FG25A121F1152IM56-B | • OFDM<br>• FSK<br>• O-QPSK | 16 dBm | 1152 | 256 | Mid | 37 | QFN56 / Standard | -40 to 125 °C |
| EFR32FG25A111F1152IM56-B | • FSK<br>• O-QPSK | 16 dBm | 1152 | 256 | Mid | 37 | QFN56 / Standard | -40 to 125 °C |
| EFR32FG25A021F512IM56-B | • OFDM<br>• FSK<br>• O-QPSK | 16 dBm | 512 | 96 | Mid | 37 | QFN56 / Standard | -40 to 125 °C |




| Field | Options |
|---|---|
| Product Family | • **EFR32FG25**: Wireless Gecko 25 Family |
| Security | • **A**: Secure Vault Mid<br>• **B**: Secure Vault High |
| Features [f1][f2][f3] | • f1<br>  • **0**: 96 KB RAM<br>  • **1**: 256 KB RAM<br>  • **2**: 512 KB RAM<br>• f2<br>  • **1**: FSK / O-QPSK<br>  • **2**: FSK / O-QPSK / OFDM<br>• f3<br>  • **1**: No feature enabled<br>  • **2**: High Quality HFCLKOUT Pin Available |
| Memory | • **F**: Flash |
| Size | • **Memory Size** in KBytes |
| Temperature Grade | • **I**: -40 to +125 °C |
| Package | • **M**: QFN |
| Pins | • **Number of Package Pins** |
| Revision | • **B**: Revision B |
| Tape & Reel | • **R**: Tape & Reel (optional) |

**Figure 2.1. Ordering Code Key**

# Table of Contents

# 3. System Overview

## 3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a high-performance radio transceiver. The devices are well suited for secure connected IoT multi-protocol devices requiring high-performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG25 Reference Manual.

A block diagram of the EFR32FG25 family is shown in Figure 3.1. Detailed EFR32FG25 Block Diagram. The diagram shows a superset of features available on the family, which vary by part number. For more information about specific device features, consult 2. Ordering Information.

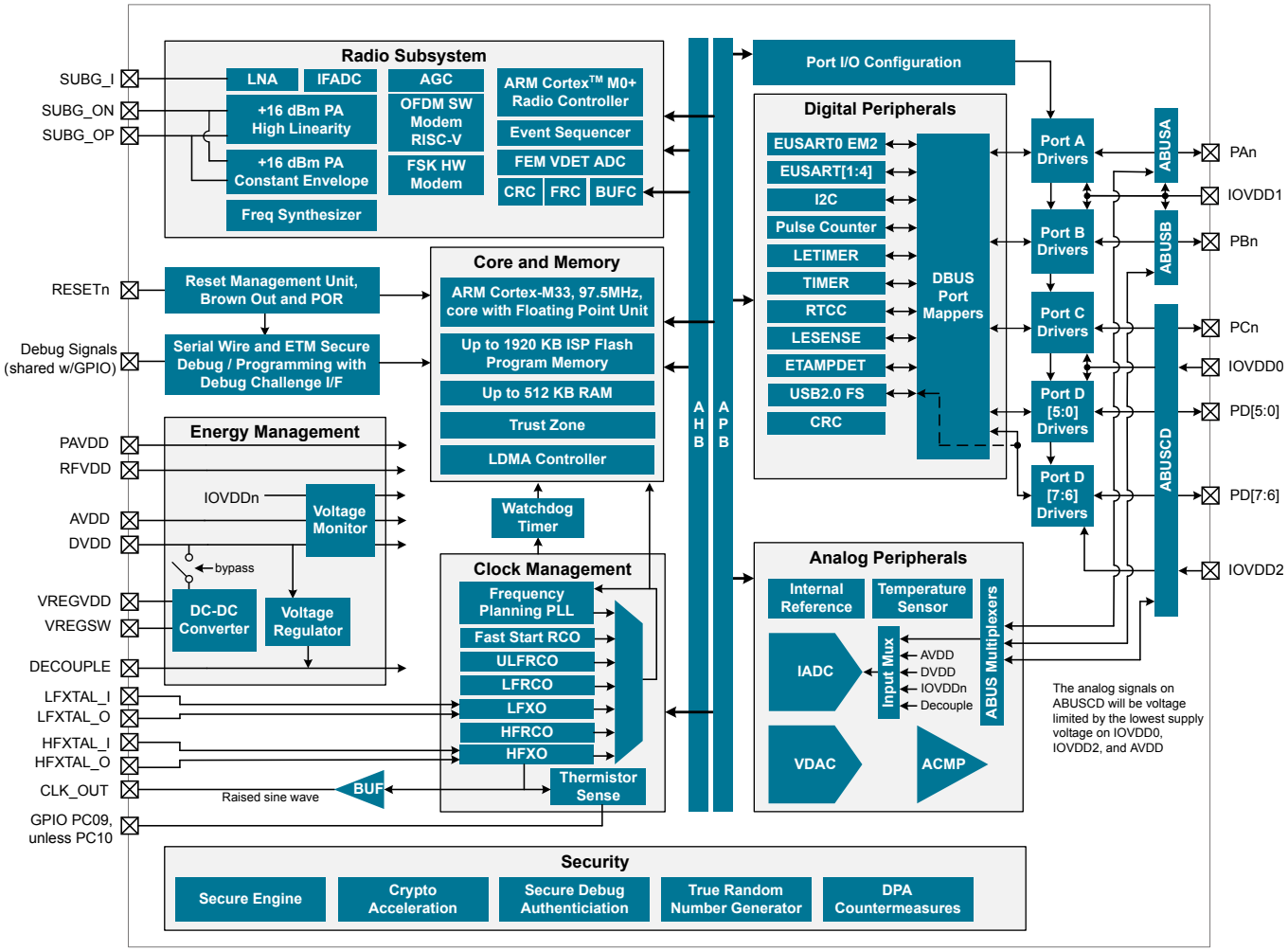



**Figure 3.1. Detailed EFR32FG25 Block Diagram**

## 3.2 Radio

The Gecko family features two radio transceivers. A hardware modem and high efficiency PA supports proprietary wireless protocols, proprietary FSK, SUN FSK, and proprietary O-QPSK. A highly configurable software defined modem and high linearity PA supports SUN O-QPSK, and SUN OFDM.

### 3.2.1 Antenna Interface

The Sub-GHz antenna is attached to an RF matching network which interfaces to a single-ended input pin (SUBG_I) that interface directly to the internal LNA input, and two differential output pins (SUBG_ON and SUBG_OP). The SUBG_ON and SUBG_OP pins interface internally to both +16 dBm differential PAs (the constant envelop high efficiency PA, and the high linearity OFDM PA). The matching networks change based on the operating frequency band.

The external components, RF matching network, and power supply connections for the typical applications are shown in later sections.

### 3.2.2 Fractional-N Frequency Synthesizer

The EFR32FG25 contains a high-performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit either as a direct modulation source for constant-envelope modulation or to provide an LO for up-conversion for other modulation schemes.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 100 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

### 3.2.3 Receiver Architecture

The EFR32FG25 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency. In some circumstances the receiver will configure with a zero IF for OFDM.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The sub-GHz radio can be calibrated on-demand by the user for the desired frequency band.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32FG25 features two demodulators, one using integrated hardware for efficient FSK reception, and other using I and Q down-converter and firmware configurable demodulator for OFDM reception. Concurrent listening for FSK and OFDM signals is supported for selected PHYs. Once a signal is detected, only one can be demodulated.

### 3.2.4 Transmitter Architecture

The EFR32FG25 uses a direct-conversion transmitter architecture with two line ups. The first is for constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping. The second is for complex modulations such as OFDM. This uses an I and Q up converter mixer, and a separate highly linear PA. The linear PA and the constant envelope PA are output on the same external pin, and can be used only one at a time.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32FG25. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

#### 3.2.5 Packet and State Trace

The EFR32FG25 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data, and state information
- Data observability on a single-pin UART data output or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data, and state / meta information in a single serial data stream

#### 3.2.6 Data Buffering

The EFR32FG25 features an advanced Radio Buffer Controller (BUFC) capable of handling up to four buffers of adjustable size from 64 to 4096 bytes. Each buffer can be used for RX, TX, or both. The buffer data is located in RAM, enabling zero-copy operations.

#### 3.2.7 Radio Controller (RAC)

The RAC controls the top-level state of the radio subsystem in the EFR32FG25. It performs the following tasks:

- Precisely timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter, and frequency synthesizer
- Detailed frame transmission timing with optional LBT or CSMA-CA

### 3.3 General Purpose Input/Output (GPIO)

EFR32FG25 supports up to 37 GPIO pins. Each GPIO pin is individually configurable as an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering are configurable on a per-pin basis. Peripheral connections can override the GPIO pins, and each peripheral connection is routeable to several GPIO pins on the device. GPIO inputs can be routed through the Peripheral Reflex System (PRS) to other peripherals. The GPIO subsystem also supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2-capable and can be used by low-energy peripherals in EM2 and EM3. These pins can also wake the device from EM2 or EM3. Pins on ports C and D retain their current state when entering EM2 until the device exits EM2, at which point internal peripherals can drive them again.

Some GPIO pins also support wake functionality down to EM4. These pins are listed in the Alternate Function Table with the function GPIO.EM4WU.

### 3.4 Clocking

#### 3.4.1 Clock Management Unit (CMU)

The CMU controls oscillators and clocks in the EFR32FG25. The CMU also enables and disables all peripheral module clocks. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

#### 3.4.2 Internal and External Oscillators

The EFR32FG25 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. The HFXO provides excellent RF clocking performance using a 39.0 MHz crystal. An integrated Thermistor Sense can accurately measure the temperature of this crystal. Internal adjustments to clock frequency can be implemented to compensate for crystal frequency shift over temperature. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature. Typical TCXO current drain and start up time are higher than the temperature compensated crystal oscillator option.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 80 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low-power operation where high accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

## 3.5 Counters/Timers and PWM

### 3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to three compare/capture channels. Each channel is configurable in one of three modes:

- In capture mode, the counter state is stored in a buffer at a selected input event.
- In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value.
- In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers.

Complementary outputs with dead-time insertion are available on select TIMER output channels.

For information on the feature set of each timer, see 3.13 Configuration Summary

### 3.5.2 Low-Energy Timer (LETIMER)

The LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. It supports timing and output generation when most of the device is powered down, allowing simple tasks to be performed while keeping system power consumption to a minimum. The LETIMER can generate a range of waveforms with minimal software involvement. The LETIMER is connected to the Peripheral Reflex System (PRS) and can start counting based on compare matches from other peripherals, such as the Real Time Clock.

### 3.5.3 System Real Time Clock with Capture (SYSRTC)

The System Real Time Clock (SYSRTC) is a 32-bit counter providing timekeeping down to EM3. The SYSRTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

### 3.5.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

### 3.5.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog and as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

## 3.6 Communications and Other Digital Peripherals

### 3.6.1 Universal Serial Bus (USB)

The optional USB on chip PHY is a full-speed/low-speed device mode USB 2.0 controller. The USB can be used in device only configurations, and uses PLL0 at 48 MHz based on the 39 MHz crystal oscillator used as reference clock for radio and MCU operation. The USB block supports both full speed (12 MBit/s) and low speed (1.5 MBit/s) operation. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 10 endpoints. Of these, 9 are Bulk endpoints which are configurable as IN or OUT or as interrupt IN endpoints, and endpoint 0 is pre-defined as CTRL IN. The on-chip PHY includes internal pull-up and pull-down resistors. Bus powered device is supported and requires external voltage regulator to supply 3.3 V to IOVDD2 whenever the system is powered. VBUS-sense requires external resistor voltage divider and uses a GPIO. USB Suspend mode, with less than 2.4 mA average current, is supported with radio receive mode at a low enough duty cycle. Radio TX is not supported in USB Suspend. Remote wakeup is supported and will use an EM2 timer.

### 3.6.2 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)

The EUSART supports full duplex asynchronous UART communication with hardware flow control, RS-485, and IrDA support. The EUSART also supports high-speed SPI. In EM0 and EM1, the EUSART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUSART0 may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud. EUSART0 can also act as a SPI secondary device in EM2 and EM3, and wake the system when data is received from an external bus controller.

### 3.6.3 Inter-Integrated Circuit Interface ($I^2C$)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$ bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode, and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the $I^2C$ module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low-energy modes. Not all instances of $I^2C$ are available in all energy modes.

### 3.6.4 Peripheral Reflex System (PRS)

The PRS provides a communication network between different peripheral modules without software involvement. Peripheral modules producing reflex signals are called producers. The PRS routes reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality, such as simple logic operations (AND, OR, NOT), can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

### 3.6.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can measure LC sensors, resistive sensors, and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

### 3.7 Secure Vault Features

A dedicated hardware secure engine containing its own CPU enables the Secure Vault functions. It isolates cryptographic functions and data from the host Cortex-M33 core, and provides several additional security features. The EFR32FG25 family includes devices with Secure Vault High and Secure Vault Mid capabilities, which are summarized in the table below.

**Table 3.1. Secure Vault Features**

| Feature | Secure Vault Mid | Secure Vault High |
|---|---|---|
| True Random Number Generator (TRNG) | Yes | Yes |
| Secure Boot with Root of Trust and Secure Loader (RTSL) | Yes | Yes |
| Secure Debug with Lock/Unlock | Yes | Yes |
| DPA Countermeasures | Yes | Yes |
| Anti-Tamper | | Yes |
| External Tamper Detect (ETAMPDET) | Yes | Yes |
| Secure Attestation | | Yes |
| Secure Key Management | | Yes |
| Symmetric Encryption | • AES 128 / 192 / 256 bit<br>  • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC | • AES 128 / 192 / 256 bit<br>  • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC<br>• ChaCha20 |
| Public Key Encryption - ECDSA / ECDH / EdDSA | • p192 and p256 | • p192, p256, p384 and p521<br>• Curve25519 (ECDH)<br>• Ed25519 (EdDSA) |
| Key Derivation | • ECJ-PAKE p192 and p256 | • ECJ-PAKE p192, p256, p384, and p521<br>• PBKDF2<br>• HKDF |
| Hashes | • SHA-1<br>• SHA-2/256 | • SHA-1<br>• SHA-2 256, 384, and 512<br>• Poly1305 |

#### 3.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over-The-Air (OTA) updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

### 3.7.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- Electronic Code Book (ECB)
- Counter Mode (CTR)
- Cipher Block Chaining (CBC)
- Cipher Feedback (CFB)
- Galois Counter Mode (GCM)
- Counter with CBC-MAC (CCM)
- Cipher Block Chaining Message Authentication Code (CBC-MAC)
- Galois Message Authentication Code (GMAC)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the National Institute of Standards and Technology (NIST) recommended curves including P-192, P-256, P-384, and P-521 for Elliptic Curve Diffie-Hellman (ECDH) key derivation, and Elliptic Curve Digital Signature Algorithm (ECDSA) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for Edwards-curve Digital Signature Algorithm (EdDSA) sign and verify operations.

Secure Vault also supports Elliptic Curve variant of Password Authenticated Key Exchange by Juggling (ECJ-PAKE) and Password-Based Key Derivation Function 2 (PBKDF2).

Supported hashes include SHA-1, SHA-2/256/384/512, and Poly1305.

This implementation provides a fast and energy-efficient solution to state of the art cryptographic needs.

### 3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31, as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

### 3.7.4 Secure Debug with Lock/Unlock

For security reasons, it is critical for a product to have its debug interface locked before being released in the field.

Secure Vault also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

### 3.7.5 Differential Power Analysis (DPA) Countermeasures

The AES and ECC accelerators have DPA countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

### 3.7.6 Secure Key Management with Physically Unclonable Function (PUF)

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a PUF to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

### 3.7.7 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, 8 external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see AN1247: Anti-Tamper Protection Configuration and Use.

### 3.7.8 External Tamper Detection (ETAMPDET)

The ETAMPDET module enables detection of external tampering, such as unauthorized enclosure opening. ETAMPDET operates in all energy modes down to EM4. Up to two signals can be generated and monitored to identify external tamper events. When a tamper event occurs, an interrupt is generated to allow software to take system-appropriate actions.

ETAMPDET is available on OPNs with Security Vault level at both Mid and High. However, only Vault High OPNs can be configured such that the Tamper block within the SE will respond autonomously to an ETAMPDET event.

### 3.7.9 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device-unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see AN1268: Authenticating Silicon Labs Devices Using Device Certificates.

## 3.8 Analog

Three analog buses route analog signals from the four GPIO ports to analog peripherals. These are ABUSA for GPIO Port A, ABUSB for GPIO Port B, and ABUSCD for GPIO Port C and Port D. The analog signals on ABUSA and ABUSB will be voltage limited by the lowest supply voltage on IOVDD1, and AVDD. The analog signals on ABUSCD will be voltage limited by the lowest supply voltage on IOVDD0, IOVDD2, and AVDD.

### 3.8.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of 12 bits at 1 Msps and 16 bits at up to 76.9 ksps. Hardware oversampling reduces system-level noise by averaging multiple front-end samples. The IADC also integrates voltage reference options and can operate in either single-ended or differential mode, with inputs selected from a wide range of internal and external sources.

### 3.8.2 Analog Comparator (ACMP)

The ACMP compares the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally programmable reference sources. The ACMP can also monitor the supply voltage and generate an interrupt when the supply falls below or rises above the programmable threshold.

### 3.8.3 Digital to Analog Converter (VDAC)

The VDAC can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

## 3.9 Power

The EFR32FG25 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFR32FG25 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

### 3.9.1 Energy Management Unit (EMU)

The EMU manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

### 3.9.2 Voltage Scaling

The EFR32FG25 supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM2 and EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level is VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM2 and EM3. The lowest level, VSCALE0, can be used to conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

### 3.9.3 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents, providing high efficiency in energy modes EM0, EM1, EM2, and EM3. RF noise mitigation allows operation of the DC-DC converter without significantly degrading sensitivity of radio components. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator via programmable software interrupt. It employs soft switching at boot and DCDC regulating-to-bypass transitions to limit the max supply slew-rate and mitigate inrush current.

### 3.9.4 Power Domains

Peripherals may exist on several independent power domains which are powered down to minimize supply current when not in use. Power domains are managed automatically by the EMU.

The lowest-energy power domain is the "high-voltage" power domain (PDHV), which supports extremely low-energy infrastructure and peripherals. Circuits powered from PDHV are always on and available in all energy modes down to EM4.

The next power domain is the low-power domain (PD0), which is further divided to power subsets of peripherals. All PD0 power domains are shut down in EM4. Circuits powered from PD0 power domains may be available in EM0, EM1, EM2, and EM3.

Low-power domain A (PD0A) is the base power domain for EM2 and EM3 and will always remain on in EM0-EM3. It powers the most commonly-used EM2 and EM3-capable peripherals and infrastructure required to operate in EM2 and EM3. Auxiliary PD0 power domains (PD0B, PD0C, PD0D, PD0E) power additional EM2 and EM3-capable peripherals on demand. If any peripherals on one of the auxiliary power domains is enabled, that power domain will be active in EM2 and EM3. Otherwise, the auxiliary PD0 power domains will be shut down to reduce current.

**Note:** Power domain PD0E is also turned on when peripherals on PD0B, PD0C, or PD0D are used.

The active power domain (PD1) powers the rest of the device circuitry, including the CPU core and EM0 / EM1 peripherals. PD1 is always powered on in EM0 and EM1. PD1 is always shut down in EM2, EM3, and EM4.

Table 3.2. Peripheral Power Subdomains shows the peripherals on the PDHV and PD0x domains. Any peripheral not listed is on PD1.

**Table 3.2. Peripheral Power Subdomains**

| Always On in EM2/EM3 | | Selectively On in EM2/3 | | | | |
|---|---|---|---|---|---|---|
| PDHV[1] | PD0A | PD0B[2] | PD0C[2] | PD0D[2] | PD0E | PDU |
| LFRCO | SYSRTC | LETIMER0 | HFRCOEM23 | DEBUG | GPIO | USB |
| LFXO | FSRCO | IADC0 | HFXO | WDOG0 | PRS | USBPLL0 |
| BURTC | | PCNT0 | | WDOG1 | | |
| BURAM | | ACMP0 | | EUSART0 | | |
| ETAMPDET | | ACMP1 | | I2C0 | | |
| ULFRCO | | LESENSE | | | | |
| | | VDAC0 | | | | |

**Note:**

1. Peripherals on PDHV are also available in EM4.
2. If any of PD0B, PD0C, or PD0D are enabled, PD0E will also be automatically enabled.

### 3.10 Reset Management Unit (RMU)

The RMU handles reset of the EFR32FG25. A wide range of reset sources are available, including several power supply monitors, pin reset, software-controlled reset, core lockup reset, and watchdog reset.

## 3.11 Core and Memory

### 3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 1920 KB flash program memory
- Up to 512 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

### 3.11.2 Memory System Controller (MSC)

The MSC is the program memory unit of the microcontroller. Both the Cortex-M33 and the LDMA can read from and write to flash memory.

In addition to the main flash array that stores program code, the MSC includes an information block. This block stores special user data and flash lock bits. It also contains a read-only page that holds system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

### 3.11.3 Linked Direct Memory Access Controller (LDMA)

The LDMA controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

### 3.12 Memory Map

The EFR32FG25 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

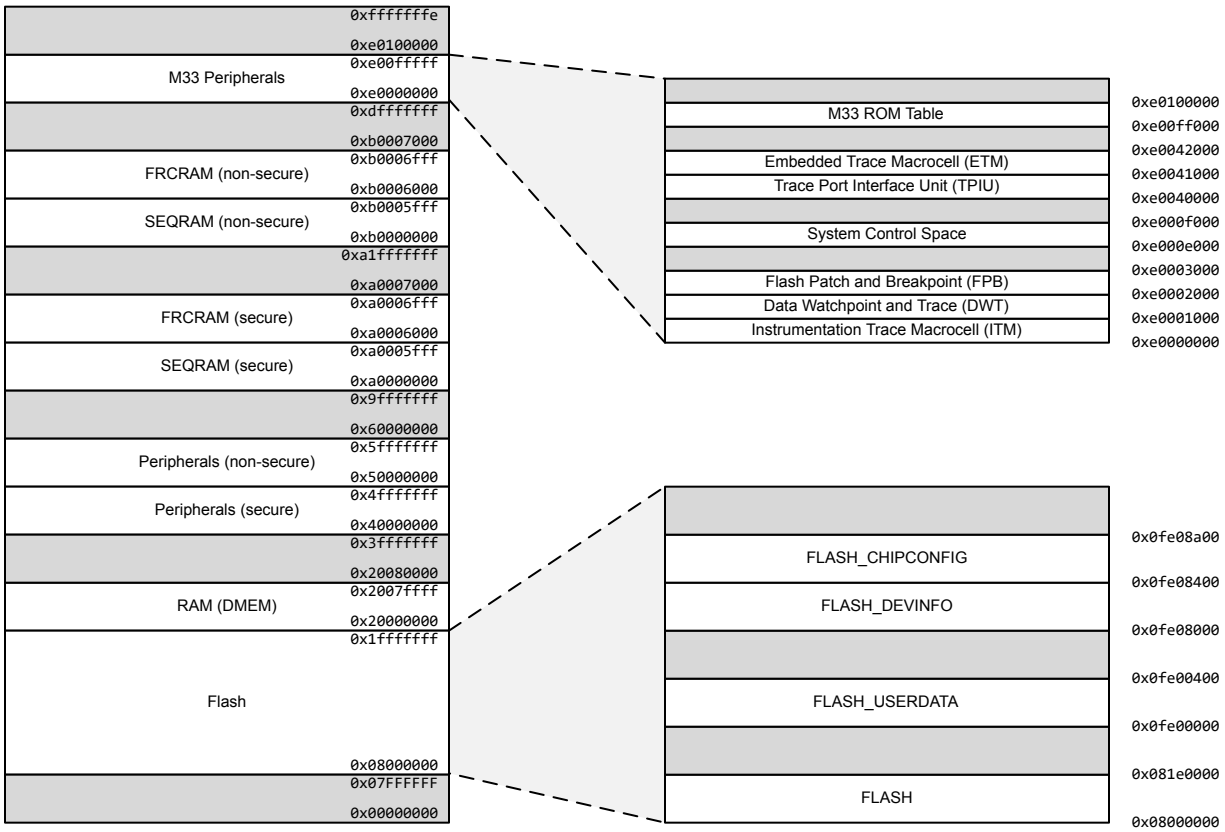



**Figure 3.2. EFR32FG25 Memory Map — Core Peripherals and Code Space**

### 3.13 Configuration Summary

The features of the EFR32FG25 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

**Table 3.3. Configuration Summary**

| Module | Lowest Energy Mode | Configuration |
|---|---|---|
| I2C0 | EM2[1] | |
| I2C1 | EM1 | |
| IADC0 | EM2 | |
| LETIMER0 | EM2[1] | 24-bit |
| TIMER0<br>TIMER1 | EM1 | 32-bit, 3-channels, +DTI |
| TIMER2<br>TIMER3<br>TIMER4<br>TIMER5<br>TIMER6 | EM1 | 16-bit, 3-channels, +DTI |
| EUSART0 | EM1 - Full high-speed operation, all modes<br>EM2[1] - Low-energy UART operation, 9600 Baud<br>EM2 or EM3[1] - Low-energy SPI secondary receiver | |
| EUSART1<br>EUSART2<br>EUSART3<br>EUSART4 | EM1 - Full high-speed operation | |

**Note:**

1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.

# 4. Electrical Specifications

## 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Devices with an output power rating of +16 dBm using the matching network corresponding to the Band of operation.
- Typical values are based on $T_A$ = 25 °C and all supplies at 3.6 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

RF electrical parameters are specified under the following additional constraints, unless stated otherwise:

- Typical (Typ) values are measured:
  - in conducted mode, based on Silicon Laboratories band-specific external RF impedance-matching networks according to Section 5.2 RF Matching Networks, and interfacing through a standard coaxial connector at the antenna port to a 50 Ω RF source for receiver tests, and 50 Ω RF Load for transmitter tests.
  - with VREGVDD = AVDD = PAVDD = 3.6 V with 0.20 Ω source resistance, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC,
  - with all MCU peripherals disabled,
  - with the reference oscillator using a 39 MHz Crystal adjusted to within ±1 ppm,
  - and with operating frequency set to $F_{RANGE}$ Typ for the specific operating band.
- Minimum (Min) and Maximum (Max) values are taken:
  - over variations in process,
  - with VREGVDD = AVDD = PAVDD adjusted together between their Min and Max voltage given in Table 4.2. General Operating Conditions
  - on operating temperature Min and Max defined in Table 4.2. General Operating Conditions under Operating ambient temperature range,
  - and on the minimum and maximum operating channel frequency between $F_{RANGE}$ Min and $F_{RANGE}$ Max for the specific operating RF Band,
  - while keeping all other conditions at typical unless otherwise noted.

Due to on-chip circuitry (e.g. diodes), some EFR32FG25 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32FG25 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VREGVDD ≥ DVDD
  - In systems using the DC-DC converter, DVDD (the buck converter output) should not be driven externally and VREGVDD (the buck converter input) must be greater than DVDD (VREGVDD > DVDD)
  - In systems not using the DC-DC converter, DVDD must be shorted to VREGVDD on the PCB (VREGVDD = DVDD)
- AVDD, IOVDD0, IOVDD1, and IOVDD2: No dependency with each other or any other supply pin. Additional leakage may occur if DVDD remains unpowered with power applied to these supplies. See Section 3.8 Analog for details on how voltage supplied to these pins affects some analog operation.
- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD

### 4.2 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

**Table 4.1. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | | -50 | — | +150 | °C |
| Voltage on any supply pin | $V_{DDMAX}$ | | -0.3 | — | 3.8 | V |
| Junction temperature | $T_{JMAX}$ | -I grade | — | — | +125 | °C |
| Voltage ramp rate on any supply pin | $V_{DDRAMPMAX}$ | | — | — | 1.0 | V / µs |
| Voltage on HFXO pins | $V_{HFXOPIN}$ | | -0.3 | — | 1.2 | V |
| DC voltage on any GPIO pin | $V_{DIGPIN}$ | | -0.3 | — | $V_{IOVDD}$ + 0.3 | V |
| DC voltage on RESETn pin[1] | $V_{RESETn}$ | | -0.3 | — | 3.8 | V |
| Total current into VDD power lines | $I_{VDDMAX}$ | Source | — | — | 200 | mA |
| Total current into VSS ground lines | $I_{VSSMAX}$ | Sink | — | — | 200 | mA |
| Current per I/O pin | $I_{IOMAX}$ | Sink | — | — | 50 | mA |
| | | Source | — | — | 50 | mA |
| Current for all I/O pins | $I_{IOALLMAX}$ | Sink | — | — | 200 | mA |
| | | Source | — | — | 200 | mA |

**Note:**

1. The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.

### 4.3 General Operating Conditions

**Table 4.2. General Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating ambient temperature range | $T_A$ | -I temperature grade [1] | -40 | — | +125 | °C |
| DVDD supply voltage | $V_{DVDD}$ | EM0/1 | 1.71 | 3.6 | 3.8 | V |
| | | EM2/3/4[2] | 1.71 | 3.6 | 3.8 | V |
| AVDD supply voltage | $V_{AVDD}$ | | 1.71 | 3.6 | 3.8 | V |
| IOVDD0 operating supply voltage | $V_{IOVDD0}$ | | 1.71 | 3.6 | 3.8 | V |
| IOVDD1 operating supply voltage | $V_{IOVDD1}$ | | 1.71 | 3.6 | 3.8 | V |
| IOVDD2 operating supply voltage | $V_{IOVDD2}$ | USB not in use | $V_{IOVDD0}$ | 3.6 | 3.8 | V |
| | | USB in use | 3.0 | 3.3 | 3.6 | V |
| RFVDD operating supply voltage | $V_{RFVDD}$ | | 1.71 | 3.6 | $V_{PAVDD}$ | V |
| PAVDD operating supply voltage | $V_{PAVDD}$ | Constant Envelope PA | 3.0 | 3.3 | 3.8 | V |
| | | OFDM 3.6 V PA | 3.45 | 3.6 | 3.8 | V |
| VREGVDD operating supply voltage | $V_{VREGVDD}$ | DCDC in bypass 60 mA load | 1.8 | 3.3 | 3.8 | V |
| | | DCDC not in use. DVDD externally shorted to VREGVDD | 1.71 | 3.3 | 3.8 | V |
| | | DCDC in regulation | 2.2 | 3.3 | 3.8 | V |
| DECOUPLE output capacitor[3] | $C_{DECOUPLE}$ | | 0.75 | 1.0 | 2.75 | µF |
| HCLK and Core frequency | $f_{HCLK}$ | VSCALE2, MODE = WS0 | — | — | 25 | MHz |
| | | VSCALE2, MODE = WS1 | — | — | 50 | MHz |
| | | VSCALE2, MODE = WS2 | — | — | 75 | MHz |
| | | VSCALE2, MODE = WS3 | — | — | 97.5 | MHz |
| PCLK frequency | $f_{PCLK}$ | VSCALE2 | — | — | 48.75 | MHz |
| EM01 Group A clock frequency | $f_{EM01GRPACLK}$ | VSCALE2 | — | — | 97.5 | MHz |
| HCLK Radio frequency[4] | $f_{HCLKRADIO}$ | VSCALE2 | — | 39.0 | 40 | MHz |
| External Clock Input | $f_{CLKIN}$ | VSCALE2, IOVDD0-2 ≥ 2.7 V | — | — | 40 | MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DPLL Reference Clock | $f_{DPLLREFCLK}$ | VSCALE2 | — | — | 40 | MHz |

**Note:**

1. The device may operate continuously at the maximum allowable ambient $T_A$ rating as long as the absolute maximum $T_{JMAX}$ is not exceeded. For an application with significant power dissipation, the allowable $T_A$ may be lower than the maximum $T_A$ rating. $T_A = T_{JMAX} - (\Theta_{JA} \times PowerDissipation)$. Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for $T_{JMAX}$ and $\Theta_{JA}$.
2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. The recommended radio crystal frequency for the sub-GHz radio is 39.0 MHz. The minimum and maximum HCLKRADIO frequency in this table represent the design timing limits, which are much wider than the typical crystal tolerance.

### 4.4 DC-DC Converter

Test conditions: $L_{DCDC}$ = 2.2 µH (Samsung CIG22H2R2MNE), $C_{DCDC}$ = 4.7 µF (TDK CGA5L3X8R1C475K160AB), $V_{VREGVDD}$ = 3.6 V, $V_{OUT}$ = 1.8 V, IPKVAL in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

**Table 4.3. DC-DC Converter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range at VREGVDD pin | $V_{VREGVDD}$ | DCDC in regulation, $I_{LOAD}$ = $I_{LOAD}$ MAX[1], EM0/EM1 mode | 2.2 | — | 3.8 | V |
| | | DCDC in regulation, $I_{LOAD}$ = 5 mA, EM0/EM1 or EM2/EM3 mode | 1.8 | — | 3.8 | V |
| | | Bypass Mode, $I_{LOAD}$ ≤ 60 mA | 1.8 | — | 3.8 | V |
| | | Bypass Mode, $I_{LOAD}$ ≤ 120 mA | 1.9 | — | 3.8 | V |
| Regulated output voltage | $V_{OUT}$ | | — | 1.8 | — | V |
| Regulation DC accuracy | $ACC_{DC}$ | $V_{VREGVDD}$ ≥ 2.2 V, Steady state in EM0/EM1 mode or EM2/EM3 mode | -2.5 | — | 4.0 | % |
| Regulation total accuracy | $ACC_{TOT}$ | All error sources (including DC errors, overshoot, undershoot) | -5 | — | 7 | % |
| Steady-state output ripple | $V_R$ | $I_{LOAD}$ = 20 mA in EM0/EM1 mode | — | 9.6 | — | mVpp |
| DC line regulation | $V_{REG}$ | $I_{LOAD}$ = $I_{LOAD}$ MAX[2]in EM0/EM1 mode, $V_{VREGVDD}$ ≥ 2.2 V | — | -2.6 | — | mV/V |
| Efficiency | EFF | Load current between 100 µA and 60 mA in EM0/EM1 mode | — | 91.4 | — | % |
| | | Load current between 10 µA and 5 mA in EM2/EM3 mode | — | 91.0 | — | % |
| DC load regulation | $I_{REG}$ | Load current between 100 µA and $I_{LOAD}$ MAX[2] in EM0/EM1 mode | — | -0.12 | — | mV/mA |
| Output load current[3] | $I_{LOAD}$ | EM0/EM1 mode, DCDC in regulation, DCDC_EM01CTRL0.IPKVAL = 9, Pulse-pairing disabled, Radio not transmitting[2] | — | — | 60 | mA |
| | | EM0/EM1 mode, DCDC in regulation, Radio in receive mode, with pulse-pairing enabled [2] | — | — | 36 | mA |
| | | EM0/EM1 mode, DCDC in regulation, Radio transmitting[1] | — | — | 120 | mA |
| | | EM2/EM3 mode, DCDC in regulation | — | — | 5 | mA |
| | | Bypass mode, 1.8 V ≤ $V_{VREGVDD}$ ≤ 3.8 V | — | — | 60 | mA |
| | | Bypass mode, 1.9 V ≤ $V_{VREGVDD}$ ≤ 3.8 V | — | — | 120 | mA |
| Nominal output capacitor | $C_{DCDC}$ | 4.7 µF ± 10% X7R capacitor used for performance characterization[4] | — | 4.7 | 10 | µF |
| Nominal inductor | $L_{DCDC}$ | ± 20% tolerance | — | 2.2 | — | µH |
| Nominal input capacitor | $C_{IN}$ | | $C_{DCDC}$ | — | — | µF |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resistance in bypass mode | $R_{BYP}$ | Bypass switch from VREGVDD to DVDD, $V_{VREGVDD}$ = 1.8 V | — | 0.46 | 0.80 | Ω |
| | | Powertrain PFET switch from VREGVDD to VREGSW, $V_{VREGVDD}$ = 1.8 V | — | 0.60 | 0.90 | Ω |
| Supply monitor threshold programming range | $V_{CMP\_RNG}$ | Programmable in 0.1 V steps | 2 | — | 2.3 | V |
| Supply monitor threshold accuracy | $V_{CMP\_ACC}$ | Supply falling edge trip point | -5 | — | 5 | % |
| Supply monitor threshold hysteresis | $V_{CMP\_HYST}$ | Positive hysteresis on the supply rising edge referred to the falling edge trip point | — | 4 | — | % |
| Supply monitor response time | $t_{CMP\_DELAY}$ | Supply falling edge at -100 mV / µs | — | 0.6 | — | µs |

**Note:**

1. During radio transmit operations, the RAIL library will place the DCDC into a mode that increases the maximum load current to support higher TX output power supplied from the DCDC converter.
2. Pulse-pairing is an optional feature to improve performance at radio frequencies below 550 MHz, but has limited output current. It is enabled by default when using RAIL with an IPKVAL setting of 3 or less. Pulse pairing may be disabled from application code by setting IPKVAL > 3. This must be done before RAIL software is initialized.
3. $I_{LOAD}$ is the total current sourced by the DCDC, including on-chip and off-chip circuits powered from the DVDD supply rail.
4. TDK CGA5L3X8R1C475K160AB used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 3.6 µF.

### 4.5 Thermal Characteristics

**Table 4.4. Thermal Characteristics**

| Package | Board | Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|---|---|
| 56QFN (7x7mm) | JEDEC - High Thermal Cond. (2s2p)[1] | Thermal Resistance, Junction to Ambient | $\Theta_{JA}$ | Still Air, JESD51-2A | 22.6 | °C/W |
| | | Thermal Resistance, Junction to Top Center | $\Psi_{JT}$ | | 0.26 | °C/W |
| | | Thermal Resistance, Junction to Board | $\Psi_{JB}$ | | 5.1 | °C/W |
| | | Thermal Resistance, Junction to Board | $\Theta_{JB}$ | JESD51-8 | 11.8 | °C/W |
| | No Board | Thermal Resistance, Junction to Case | $\Theta_{JC}$ | Temperature controlled heat sink on top of package, all other sides of package insulated to prevent heat flow, per JESD51-14 | 2.0 | °C/W |

**Note:**

1. Based on 4 layer PCB with dimension 76 mm x 110 mm, PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 25 Via to top internal plane of PCB.

## 4.6 Current Consumption

### 4.6.1 MCU Current Consumption Using DC-DC at 3.6 V Input

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = PAVDD = 3.6 V. DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE2. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.5. MCU Current Consumption Using DC-DC at 3.6 V Input**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled | $I_{ACTIVE}$ | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal, CPU running Prime from flash | — | 31 | — | µA/MHz |
| | | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal, CPU running while loop from flash | — | 30 | — | µA/MHz |
| | | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal, CPU running CoreMark loop from flash | — | 43 | — | µA/MHz |
| | | 39.0 MHz crystal, CPU running Prime from flash | — | 35 | — | µA/MHz |
| | | 39.0 MHz crystal, CPU running while loop from flash | — | 35 | — | µA/MHz |
| | | 39.0 MHz crystal, CPU running CoreMark loop from flash | — | 49 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 30 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 34 | — | µA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 43 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 395 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | $I_{EM1}$ | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal | — | 22 | — | µA/MHz |
| | | 39.0 MHz crystal | — | 26 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 21 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 25 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 34 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 386 | — | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM2 mode, VSCALE0 | $I_{EM2\_VS}$ | Full RAM retention and RTC running from LFXO | — | 4.6 | — | µA |
| | | Full RAM retention and RTC running from LFRCO | — | 4.6 | — | µA |
| | | Full RAM retention and RTC running from LFRCO with USB connected and in Suspend mode with IOVDD2 = 3.3 V | — | 7.0 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO | — | 2.6 | — | µA |
| | | 32 KB RAM retention and RTC running from LFRCO | — | 2.6 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO, Sequencer RAM and CPU cache not retained | — | 2.3 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO, Sequencer RAM, CPU cache, and EM0/1 peripheral states not retained | — | 2.3 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO, Sequencer RAM, FRC RAM, CPU cache, and EM0/1 peripheral states not retained | — | 2.3 | — | µA |
| Current consumption in EM3 mode, VSCALE0 | $I_{EM3\_VS}$ | 32 KB RAM retention and RTC running from ULFRCO | — | 2.4 | — | µA |
| Current consumption for retained RAM bank in EM2 or EM3 | $I_{RAM}$ | Per 32 KB RAM bank | — | 0.13 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1] | $I_{PD0B\_VS}$ | | — | 0.37 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0C is enabled[1] | $I_{PD0C\_VS}$ | | — | 0.06 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0D is enabled[1] | $I_{PD0D\_VS}$ | | — | 0.58 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0E is enabled[1] | $I_{PD0E\_VS}$ | | — | 0.07 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PDU is enabled[1] | $I_{PDU\_VS}$ | | — | 1.42 | — | µA |

**Note:**

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.

### 4.6.2 MCU Current Consumption at 3.6 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = IOVDD0-2 = 3.6 V. DC-DC not used. Voltage scaling level = VSCALE2. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.6. MCU Current Consumption at 3.6 V**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled | $I_{ACTIVE}$ | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal, CPU running Prime from flash | — | 53 | — | µA/MHz |
| | | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal, CPU running while loop from flash | — | 53 | — | µA/MHz |
| | | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal, CPU running CoreMark loop from flash | — | 75 | — | µA/MHz |
| | | 39.0 MHz crystal, CPU running Prime from flash | — | 61 | — | µA/MHz |
| | | 39.0 MHz crystal, CPU running while loop from flash | — | 60 | — | µA/MHz |
| | | 39.0 MHz crystal, CPU running CoreMark loop from flash | — | 86 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 52 | 97 | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 60 | — | µA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 76 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 685 | 2300 | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | $I_{EM1}$ | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal | — | 38 | — | µA/MHz |
| | | 39.0 MHz crystal | — | 45 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 36 | 80 | µA/MHz |
| | | 26 MHz HFRCO | — | 44 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 60 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 669 | 2200 | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM2 mode, VSCALE0 | $I_{EM2\_VS}$ | Full RAM retention and RTC running from LFXO | — | 7.9 | — | µA |
| | | Full RAM retention and RTC running from LFRCO | — | 8.0 | 20 | µA |
| | | Full RAM retention and RTC running from LFRCO with USB connected and in Suspend mode with IOVDD2 = 3.3 V | — | 10.4 | — | µA |
| | | 32 KB RAM retention and RTC running from LFRCO | — | 4.4 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO | — | 4.4 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO, Sequencer RAM and CPU cache not retained | — | 3.9 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO, Sequencer RAM, CPU cache, and EM0/1 peripheral states not retained | — | 3.9 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO, Sequencer RAM, FRC RAM, CPU cache, and EM0/1 peripheral states not retained | — | 3.8 | — | µA |
| Current consumption in EM3 mode, VSCALE0 | $I_{EM3\_VS}$ | Full RAM retention and RTC running from ULFRCO | — | 7.6 | — | µA |
| | | 32 KB RAM retention and RTC running from ULFRCO | — | 4.0 | 9.0 | µA |
| Current consumption for retained RAM bank in EM2 or EM3 | $I_{RAM}$ | Per 32 KB RAM bank | — | 0.24 | — | µA |
| Current consumption in EM4 mode | $I_{EM4}$ | No BURTC, no LF oscillator | — | 0.74 | 1.50 | µA |
| | | BURTC with LFXO | — | 1.14 | — | µA |
| | | ETAMPDET active[1] | — | 0.87 | — | µA |
| Current consumption during reset | $I_{RST}$ | Hard pin reset held | — | 482 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[2] | $I_{PD0B\_VS}$ | | — | 0.61 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0C is enabled[2] | $I_{PD0C\_VS}$ | | — | 0.08 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0D is enabled[2] | $I_{PD0D\_VS}$ | | — | 0.97 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0E is enabled[2] | $I_{PD0E\_VS}$ | | — | 0.09 | — | µA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Additional current in EM2 or EM3 when any peripheral in PDU is enabled[2] | $I_{PDU\_VS}$ | | — | 2.5 | — | µA |

**Note:**

1. ETAMPDET operating from ULFRCO divided down to 100 Hz, with 1 nF load capacitance to ground.
2. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.

### 4.6.3 MCU Current Consumption at 3.3 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = IOVDD0-2 = 3.3 V. DC-DC not used. Voltage scaling level = VSCALE2. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.7. MCU Current Consumption at 3.3 V**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled | $I_{ACTIVE}$ | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal, CPU running Prime from flash | — | 53 | — | µA/MHz |
| | | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal, CPU running while loop from flash | — | 53 | — | µA/MHz |
| | | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal, CPU running CoreMark loop from flash | — | 75 | — | µA/MHz |
| | | 39.0 MHz crystal, CPU running Prime from flash | — | 61 | — | µA/MHz |
| | | 39.0 MHz crystal, CPU running while loop from flash | — | 60 | — | µA/MHz |
| | | 39.0 MHz crystal, CPU running CoreMark loop from flash | — | 86 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 52 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 59 | — | µA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 75 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 684 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | $I_{EM1}$ | 97.5 MHz RFFPLL referenced to 39.0 MHz crystal | — | 39 | — | µA/MHz |
| | | 39.0 MHz crystal | — | 45 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 36 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 44 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 60 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 668 | — | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM2 mode, VSCALE0 | $I_{EM2\_VS}$ | Full RAM retention and RTC running from LFXO | — | 7.6 | — | µA |
| | | Full RAM retention and RTC running from LFRCO | — | 7.6 | — | µA |
| | | Full RAM retention and RTC running from LFRCO with USB connected and in Suspend mode with IOVDD2 = 3.3 V | — | 10 | — | µA |
| | | 32 KB RAM retention and RTC running from LFRCO | — | 4.1 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO | — | 4.0 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO, Sequencer RAM and CPU cache not retained | — | 3.6 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO, Sequencer RAM, CPU cache, and EM0/1 peripheral states not retained | — | 3.6 | — | µA |
| | | 32 KB RAM retention and RTC running from LFXO, Sequencer RAM, FRC RAM, CPU cache, and EM0/1 peripheral states not retained | — | 3.5 | — | µA |
| Current consumption in EM3 mode, VSCALE0 | $I_{EM3\_VS}$ | Full RAM retention and RTC running from ULFRCO | — | 7.2 | — | µA |
| | | 32 KB RAM retention and RTC running from ULFRCO | — | 3.7 | — | µA |
| Current consumption for retained RAM bank in EM2 or EM3 | $I_{RAM}$ | Per 32 KB RAM bank | — | 0.23 | — | µA |
| Current consumption in EM4 mode | $I_{EM4}$ | No BURTC, no LF oscillator | — | 0.40 | — | µA |
| | | BURTC with LFXO | — | 0.81 | — | µA |
| | | ETAMPDET active[1] | — | 0.54 | — | µA |
| Current consumption during reset | $I_{RST}$ | Hard pin reset held | — | 468 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[2] | $I_{PD0B\_VS}$ | | — | 0.62 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0C is enabled[2] | $I_{PD0C\_VS}$ | | — | 0.10 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0D is enabled[2] | $I_{PD0D\_VS}$ | | — | 0.98 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0E is enabled[2] | $I_{PD0E\_VS}$ | | — | 0.11 | — | µA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Additional current in EM2 or EM3 when any peripheral in PDU is enabled[2] | $I_{PDU\_VS}$ | | — | 2.5 | — | µA |

**Note:**

1. ETAMPDET operating from ULFRCO divided down to 100 Hz, with 1 nF load capacitance to ground.
2. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.

### 4.6.4 Radio Current Consumption with DC-DC at 3.3 V Input

RF current consumption measured with MCU in EM1, HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = PAVDD = 3.3 V. DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.8. Radio Current Consumption with DC-DC at 3.3 V Input**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in receive mode, active packet reception, VSCALE2, EM1P[1] | $I_{RX\_ACTIVE}$ | f = 915 MHz, O-QPSK, 4.8 kbps | — | 5.8 | — | mA |
| | | f = 924 MHz, 4-GFSK, 400 kbps | — | 6.3 | — | mA |
| | | f = 868 MHz, 2-GFSK, 38.4 kbps | — | 5.7 | — | mA |
| | | f = 868 MHz, GMSK, 500 kbps | — | 6.3 | — | mA |
| | | f = 868 MHz, O-QPSK, 100 kbps | — | 6.3 | — | mA |
| | | f = 915 MHz, O-QPSK, 250 kbps | — | 8.8 | — | mA |
| Current consumption in receive mode, listening for packet, VSCALE2, EM1P[1] | $I_{RX\_LISTEN}$ | f = 915 MHz, O-QPSK, 4.8 kbps | — | 5.7 | — | mA |
| | | f = 924 MHz, 4-GFSK, 400 kbps | — | 6.4 | — | mA |
| | | f = 868 MHz, 2-GFSK, 38.4 kbps | — | 5.7 | — | mA |
| | | f = 868 MHz, GMSK, 500 kbps | — | 6.3 | — | mA |
| | | f = 868 MHz, O-QPSK, 100 kbps | — | 6.4 | — | mA |
| | | f = 915 MHz, O-QPSK, 250 kbps | — | 9.1 | — | mA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in transmit mode, VSCALE2, EM1 | $I_{TX}$ | f = 915 MHz, CW, PAVDD[2] = 3.3 V, 0 dBm output power[3] | — | 24.9 | — | mA |
| | | f = 915 MHz, CW, PAVDD[2] = 3.6 V, 0 dBm output power[3] | — | 24.7 | — | mA |
| | | f = 915 MHz, CW, PAVDD[2] = 3.3 V, 12 dBm output power[3] | — | 54.5 | — | mA |
| | | f = 915 MHz, CW, PAVDD[2] = 3.6 V, 12 dBm output power[3] | — | 54.3 | — | mA |
| | | f = 915 MHz, CW, PAVDD[2] = 3.3 V, $POUT_{MAX}$[4] output power[3] | — | 76.8 | — | mA |
| | | f = 915 MHz, CW, PAVDD[2] = 3.6 V, $POUT_{MAX}$[4] output power[3] | — | 76.6 | — | mA |
| | | f = 924 MHz, CW, PAVDD[2] = 3.3 V, 13 dBm output power[3] | — | 58.8 | — | mA |
| | | f = 924 MHz, CW, PAVDD[2] = 3.6 V, 13 dBm output power[3] | — | 58.6 | — | mA |
| | | f = 868 MHz, CW, PAVDD[2] = 3.3 V, 14 dBm output power[3] | — | 52.0 | — | mA |
| | | f = 470 MHz, CW, PAVDD[2] = 3.3 V, 16 dBm output power[5] | — | 72.8 | — | mA |

**Note:**

1. EM1P operation is 0.22 mA lower than EM1 operation
2. VREGVDD and AVDD tied to PAVDD
3. Using the 868/915/920 MHz matching network as shown in the typical connections section.
4. Same $POUT_{MAX}$ setting as in Table 4.14. 915 MHz Band +16 dBm RF Constant Envelope Transmitter Characteristics
5. Using the 470 MHz matching network as shown in the typical connections section.

### 4.6.5 SUN O-QPSK Radio Current Consumption with DC-DC at 3.3 V Input

SUN O-QPSK DSSS Modulations are defined by IEEE 802.15.4-2020 section 21, and Table 21-4 using the following abbreviations: f = operating frequency (MHz), Rc = baud or Chip rate (kchip/s), RM = Rate mode (index), Rd = Data bit rate (kbps), and PL = PSDU Length (octets). Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = PAVDD = 3.3 V. DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.9. SUN O-QPSK Radio Current Consumption with DC-DC at 3.3 V Input**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in SUN O-QPSK Receive mode, active packet reception, VSCALE2, EM1P | $I_{RX\_ACTIVE}$ | f = 914, Rc = 100, RM = 0, Rd = 6.25, PL = 20 | — | 6.6 | — | mA |
| | | f = 914, Rc = 100, RM = 2, Rd = 25, PL = 20 | — | 6.6 | — | mA |
| | | f = 914, Rc = 100, RM = 3, Rd = 50, PL = 250 | — | 6.7 | — | mA |
| | | f = 914, Rc = 1000, RM = 0, Rd = 31.25, PL = 20 | — | 8.2 | — | mA |
| | | f = 914, Rc = 1000, RM = 3, Rd = 500, PL = 250 | — | 8.6 | — | mA |
| Current consumption in SUN O-QPSK Receive mode, listening for indicated modulation with no input signal, VSCALE2, EM1P | $I_{RX\_LISTEN}$ | f = 914, Rc = 100, RM = 0, Rd = 6.25, PL = 20 | — | 6.8 | — | mA |
| | | f = 914, Rc = 100, RM = 2, Rd = 25, PL = 20 | — | 6.8 | — | mA |
| | | f = 914, Rc = 100, RM = 3, Rd = 50, PL = 250 | — | 6.8 | — | mA |
| | | f = 914, Rc = 1000, RM = 0, Rd = 31.25, PL = 20 | — | 8.9 | — | mA |
| | | f = 914, Rc = 1000, RM = 3, Rd = 500, PL = 250 | — | 8.9 | — | mA |
| Current consumption in SUN O-QPSK transmit mode at $POUT_{MAX}$[1] output power | $I_{TXPOUT\_MAX}$ | f = 914, Rc = 100, RM = 2, Rd = 25, PL = 20 | — | 71.6 | — | mA |

**Note:**

1. Same $POUT_{MAX}$ setting as in Table 4.14. 915 MHz Band +16 dBm RF Constant Envelope Transmitter Characteristics

### 4.6.6 SUN OFDM Radio Current Consumption with DC-DC at 3.6 V Input

These radio current consumption measurements for Min and Max use the same transceiver settings as the Typ. Measurements use packet length of 250 octets when data rate is 50 kbps or higher, and 20 octets packet length when lower then 50 kbps. OFDM Modulation is defined in 802.15.4-2020 section 20.3 . In this table, f = operating frequency in MHz, and the indication "OptX, MCSy" means X as the Option number 1 through 4, and y is the MCS index 0 through 6, and PL = PSDU Length (octets). Unless otherwise indicated, conditions are: VREGVDD = AVDD = PAVDD = 3.6 V. DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC. $T_A$ = 25 °C.

**Table 4.10. SUN OFDM Radio Current Consumption with DC-DC at 3.6 V Input**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in SUN OFDM Receive mode, active packet reception, VSCALE2, EM1P | $I_{RX\_ACTIVE}$ | f = 914, Opt1, MCS2 | — | 8.6 | — | mA |
| | | f = 914, Opt1, MCS6, $T_A$ = 25 °C[1] | — | 8.6 | 9.0 | mA |
| | | f = 914, Opt2, MCS3 | — | 7.7 | — | mA |
| | | f = 914, Opt2, MCS6 | — | 7.8 | — | mA |
| | | f = 923.7, Opt3, MCS4, $T_A$ = 25 °C[1] | — | 8.9 | 9.4 | mA |
| | | f = 923.7, Opt3, MCS5 | — | 8.8 | — | mA |
| | | f = 923.7, Opt3, MCS6 | — | 8.8 | — | mA |
| | | f = 866.5, Opt4, MCS4 | — | 8.7 | — | mA |
| | | f = 866.5, Opt4, MCS6 | — | 8.6 | — | mA |
| Current consumption in SUN OFDM Receive mode, listening for indicated modulation with no input signal, VSCALE2, EM1P | $I_{RX\_LISTEN}$ | f = 914, Opt1, MCS2 | — | 8.2 | — | mA |
| | | f = 914, Opt1, MCS6, $T_A$ = 25 °C[1] | — | 8.2 | 8.6 | mA |
| | | f = 914, Opt2, MCS3 | — | 7.4 | — | mA |
| | | f = 914, Opt2, MCS6 | — | 7.4 | — | mA |
| | | f = 923.7, Opt3, MCS4, $T_A$ = 25 °C[1] | — | 7.2 | 7.7 | mA |
| | | f = 923.7, Opt3, MCS5 | — | 7.2 | — | mA |
| | | f = 923.7, Opt3, MCS6 | — | 7.2 | — | mA |
| | | f = 866.5, Opt4, MCS4 | — | 7.2 | — | mA |
| | | f = 866.5, Opt4, MCS6 | — | 7.2 | — | mA |
| Current consumption in SUN OFDM transmit mode with average TX output power set to 16 dBm | $I_{TX16}$ | f = 914, Opt1, MCS2, $T_A$ = 25 °C[1] | — | 187 | 194 | mA |
| | | f = 914, Opt1, MCS3 | — | 187 | — | mA |
| | | f = 914, Opt1, MCS6 | — | 186 | — | mA |
| | | f = 914, Opt2, MCS3 | — | 186 | — | mA |
| | | f = 914, Opt2, MCS6 | — | 186 | — | mA |
| | | f = 490, Opt4, MCS6 | — | 189 | — | mA |
| Current consumption in SUN OFDM transmit mode with average TX output power set to 14 dBm | $I_{TX14}$ | f = 866.5, Opt4, MCS4 | — | 184 | — | mA |
| | | f = 866.5, Opt4, MCS6 | — | 184 | — | mA |
| Current consumption in SUN OFDM transmit mode with average TX output power set to 13 dBm | $I_{TX13}$ | f = 923.7, Opt3, MCS4, $T_A$ = 25 °C[1] | — | 184 | 191 | mA |
| | | f = 923.7, Opt3, MCS5 | — | 184 | — | mA |
| | | f = 923.7, Opt3, MCS6, $T_A$ = 25 °C[1] | — | 184 | 191 | mA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in SUN OFDM transmit mode at 12 dBm average | $I_{TX12}$ | f = 914, Opt1, MCS2 | — | 184 | — | mA |
| | | f = 914, Opt1, MCS6 | — | 184 | — | mA |
| | | f = 914, Opt2, MCS3 | — | 184 | — | mA |
| | | f = 914, Opt2, MCS6 | — | 184 | — | mA |
| | | f = 923.7, Opt3, MCS4 | — | 184 | — | mA |
| | | f = 923.7, Opt3, MCS5 | — | 184 | — | mA |
| | | f = 923.7, Opt3, MCS6 | — | 184 | — | mA |
| | | f = 866.5, Opt4, MCS4 | — | 183 | — | mA |
| | | f = 866.5, Opt4, MCS6 | — | 183 | — | mA |
| Current consumption in SUN OFDM transmit mode at 0 dBm average output power with VREGVDD = AVDD = PAVDD = 3.3 V | $I_{TX0}$ | f = 914, Opt1, MCS2 | — | 70.3 | — | mA |
| | | f = 914, Opt1, MCS6 | — | 70.1 | — | mA |
| | | f = 914, Opt2, MCS3 | — | 70.0 | — | mA |
| | | f = 914, Opt2, MCS6 | — | 69.9 | — | mA |
| | | f = 923.7, Opt3, MCS4 | — | 69.8 | — | mA |
| | | f = 923.7, Opt3, MCS5 | — | 69.8 | — | mA |
| | | f = 923.7, Opt3, MCS6 | — | 69.7 | — | mA |
| | | f = 866.5, Opt4, MCS4 | — | 69.9 | — | mA |
| | | f = 866.5, Opt4, MCS6 | — | 69.9 | — | mA |

**Note:**

1. For a detailed characteristic over temperature see Figure 4.5. Typical Radio Supply Current and Output Power vs. Temperature

### 4.7 Energy Mode Wake-up and Entry Time

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz, with the DPLL disabled.

**Table 4.11. Energy Mode Wake-up and Entry Time**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Wake-up time from EM1 | $t_{EM1\_WU}$ | Code execution from flash | — | 3 | — | HCLKs |
| | | Code execution from RAM | — | 1.43 | — | µs |
| Wake-up time from EM2 | $t_{EM2\_WU}$ | Code execution from flash, no voltage scaling | — | 12.2 | — | µs |
| | | Code execution from RAM, no voltage scaling | — | 5.4 | — | µs |
| | | Voltage scaling up one level[1] | — | 36.9 | — | µs |
| | | Voltage scaling up two levels[2] | — | 49.2 | — | µs |
| Wake-up time from EM3 | $t_{EM3\_WU}$ | Code execution from flash, no voltage scaling | — | 12.2 | — | µs |
| | | Code execution from RAM, no voltage scaling | — | 5.4 | — | µs |
| | | Voltage scaling up one level[1] | — | 36.9 | — | µs |
| | | Voltage scaling up two levels[2] | — | 49.2 | — | µs |
| Wake-up time from EM4 | $t_{EM4\_WU}$ | Code execution from flash | — | 24.3 | — | ms |
| Entry time to EM1 | $t_{EM1\_ENT}$ | Code execution from flash | — | 1.13 | — | µs |
| Entry time to EM2 | $t_{EM2\_ENT}$ | Code execution from flash | — | 5.4 | — | µs |
| Entry time to EM3 | $t_{EM3\_ENT}$ | Code execution from flash | — | 5.4 | — | µs |
| Entry time to EM4 | $t_{EM4\_ENT}$ | Code execution from flash | — | 10.8 | — | µs |

**Note:**

1. Voltage scaling one level is between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.

### 4.8 Flash Characteristics

**Table 4.12. Flash Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Flash Supply voltage during write or erase | $V_{FLASH}$ | | 1.71 | — | 3.8 | V |
| Flash erase cycles before failure[1] | $EC_{FLASH}$ | $T_A \leq 125$ °C | 10,000 | — | — | cycles |
| Flash data retention[1] | $RET_{FLASH}$ | $T_A \leq 125$ °C | 10 | — | — | years |
| Program Time | $t_{PROG}$ | one word (32-bits) | 40.4 | 44.3 | 48.1 | µs |
| | | average per word over 128 words | 10.4 | 11.4 | 12.5 | µs |
| Page Erase Time | $t_{PERASE}$ | | 11.8 | 13.3 | 14.6 | ms |
| Mass Erase Time | $t_{MERASE}$ | 1920 KB | 177 | 189 | 219 | ms |
| | | 1152 KB | 106 | 113 | 132 | ms |
| Program Current | $I_{PROG}$ | | — | — | 2.9 | mA |
| Page Erase Current | $I_{PERASE}$ | Page Erase | — | — | 1.8 | mA |
| Mass Erase Current | $I_{MERASE}$ | Mass Erase | — | — | 1.9 | mA |

**Note:**

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.

## 4.9 Sub-GHz RF Transceiver Characteristics

### 4.9.1 RF Constant Envelope Transmitter Characteristics

#### 4.9.1.1 920 MHz Band +13 dBm RF Constant Envelope Transmitter Characteristics

This table is for devices with an output power rating of +16 dBm using the 868/915/920 MHz matching network as shown in the typical connections section. Band is 922.3 to 928.1 MHz. Emissions are measured at 13 dBm and 0 dBm. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, crystal frequency = 39.0 MHz, supply filtering as shown in the typical connections section, and RF center frequency 924 MHz.

**Table 4.13. 920 MHz Band +13 dBm RF Constant Envelope Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 922.3 | 924 | 928.1 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | 16 dBm devices, matching network as shown in the typical connections section[1 2 3] | 11.4 | 13.4 | 16.1 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -39.4 | -38.9 | dBm |
| Output power variation vs supply | $POUT_{VAR\_V}$ | 3.0 V < VREGVDD = AVDD = PAVDD < 3.8 V, T = 25 °C at 13 dBm nominal settings | — | 0.02 | 0.1 | dB |
| | | 3.0 V < VREGVDD = AVDD = PAVDD < 3.8 V, T = 25 °C at 0 dBm nominal settings | — | 0.02 | 0.1 | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR\_T}$ | $T_A$ = -40 to +85 °C, VREGVDD = AVDD = PAVDD = 3.3 V, and 13 dBm nominal settings. | — | 0.7 | 1.5 | dB |
| | | $T_A$ = -40 to +125 °C. VREGVDD = AVDD = PAVDD = 3.3 V, and 13 dBm nominal settings. | — | 0.9 | 2.1 | dB |
| Output power variation vs RF frequency | $POUT_{VAR\_F}$ | VREGVDD = AVDD = PAVDD = 3.3 V, $T_A$ = 25 °C | — | 0.02 | 0.13 | dB |
| Adjacent Channel Power 50 kbps 2FSK[3 4] | $P_{CH\_ADJ\_50}$ | $P_{OUT}$ = 0 dBm (1 mW), 924 MHz, 200 kHz channel spacing | — | -29.0 | -26.0 | dBm |
| | | $P_{OUT}$ = 13 dBm (20 mW), 924 MHz, 200 kHz channel spacing[5] | — | -15.7 | -15.0 | dBm |
| Adjacent Channel Power 100 kbps 2FSK[3 6] | $P_{CH\_ADJ\_100}$ | $P_{OUT}$ = 0 dBm (1 mW), 924 MHz, 400 kHz channel spacing | — | -30.4 | -26.0 | dBm |
| | | $P_{OUT}$ = 13 dBm (20 mW), 924 MHz, 400 kHz channel spacing | — | -17.1 | -15.0 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max spurious emissions, $P_{OUT}$ = 0 dBm (1 mW)[3] [4] with VREGVDD = PAVDD = AVDD = 3.0 V | $SPUR_{TX\_ARIB\_0}$ | f ≤ 710 MHz, RBW = 100 kHz | — | -77.1 | -36.0 | dBm |
| | | 710 MHz < f ≤ 900 MHz, RBW = 1 MHz | — | -69.4 | -55.0 | dBm |
| | | 900 MHz < f ≤ 915 MHz, RBW = 100 kHz | — | -78.3 | -55.0 | dBm |
| | | 915 MHz < f ≤ 930 MHz, RBW = 100 kHz, (except for \|f-fc\| ≤ (200+100*n) kHz) | — | -48.8 | -36.0 | dBm |
| | | 930 MHz < f ≤ 1000 MHz, RBW = 100 kHz | — | -75.2 | -55.0 | dBm |
| | | 1000 MHz < f ≤ 1215 MHz, RBW = 1 MHz | — | -67.4 | -45.0 | dBm |
| | | 1215 MHz < f, RBW = 1 MHz | — | -59.2 | -30.0 | dBm |
| Max spurious emissions, $P_{OUT}$ = 13 dBm (20 mW)[3] [4] | $SPUR_{TX\_ARIB\_13}$ | f ≤ 710 MHz, RBW = 100 kHz | — | -66.8 | -36.0 | dBm |
| | | 710 MHz < f ≤ 900 MHz, RBW = 1 MHz | — | -56.5 | -55.0 | dBm |
| | | 900 MHz < f ≤ 915 MHz, RBW = 100 kHz | — | -65.3 | -55.0 | dBm |
| | | 915 MHz < f ≤ 930 MHz, RBW = 100 kHz, (except for \|f-fc\| ≤ (200+100*n) kHz)[7] | — | -40.9 | -36.0 | dBm |
| | | 930 MHz < f ≤ 1000 MHz, RBW = 100 kHz | — | -62.9 | -55.0 | dBm |
| | | 1000 MHz < f ≤ 1215 MHz, RBW = 1 MHz | — | -56.1 | -45.0 | dBm |
| | | 1215 MHz < f, RBW = 1 MHz | — | -48.0 | -30.0 | dBm |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.
2. The transmit power for the 922.3 to 928.1 Band MHz is normally limited by regulatory agency to +13 dBm (20 mW). The 16 dBm devices are recommended with the matching network as shown in the typical connections section.
3. The matching network shown in the typical connections section is optimized for best efficiency at 16 dBm. The maximum output power can be above the maximum rating in certain conditions. Emissions for this band are tested at $T_A$ = 25 °C with the output power set to 13 dBm (20 mW) and 0 dBm (1mW).
4. Measured per ARIB T108, Part 2 Section 3.2,$f_c$ = 924 MHz, 922.3 to 928.1 frequency band, 50 kbps, 2FSK, BT = 2, Δf = ± 25 kHz, PN9 sequence, 200 kHz channel spacing, n = 1.
5. The margin to the regulatory limit (-15 dBm) can be increased by selecting lower BT product values. Example settings and resulting margins can be seen in the following table:

| BT Product | $P_{CH\_ADJ\_50}$ [dBm] | Margin [dB] |
|---|---|---|
| 2 | -15.7 | 0.7 |
| 1.3 | -20 | 5 |
| 1.0 | -25 | 10 |
| 0.5 | -30 | 15 |

6. Measured per ARIB T108, Part 2 Section 3.2,$f_c$ = 924 MHz, 922.3 to 928.1 frequency band, 100 kbps, 2FSK, BT = 2, Δf = ± 25 kHz, PN9 sequence, 400 kHz channel spacing, n = 2.
7. The spurious emission is calculated according to TELEC-T245 5th Ed. Spurious Emissions Measurement Procedure Section 4 (6) to (16)

#### 4.9.1.2 915 MHz Band +16 dBm RF Constant Envelope Transmitter Characteristics

This table is for devices with an output power rating of +16 dBm using the 868/915/920 MHz matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, crystal frequency = 39.0 MHz, supply filtering as shown in the typical connections section, and RF center frequency 915 MHz.

**Table 4.14. 915 MHz Band +16 dBm RF Constant Envelope Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | 915 | 928 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | 16 dBm devices, matching network as shown in the typical connections section[1] [2] | 14.2 | 15.9 | 18.4 | dBm |
| Minimum active TX power | $POUT_{MIN}$ | | — | -39.5 | -38.3 | dBm |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR\_V}$ | 3.0 V < VREGVDD = AVDD = PAVDD < 3.8 V, T = 25 °C, and at 16 dBm nominal settings | — | 0.03 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR\_T}$ | $T_A$ = -40 to +85 °C with VREGVDD = AVDD = PAVDD = 3.3 V, and 16 dBm nominal settings. | — | 0.8 | — | dB |
| | | $T_A$ = -40 to +125 °C with VREGVDD = AVDD = PAVDD = 3.3 V, and 16 dBm nominal settings. | — | 1.0 | — | dB |
| Output power variation vs RF frequency | $POUT_{VAR\_F}$ | VREGVDD = AVDD = PAVDD = 3.3 V, 16 dBm nominal settings, and $T_A$ = 25 °C | — | 0.05 | — | dB |
| Spurious emissions of harmonics, Conducted measurement, Test Frequency = 915 MHz[2] | $SPUR_{HARM\_FCC}$ | In non-restricted bands, per FCC 47 CFR §15.247[3] | — | -62.2 | -20.0 | dBc |
| | | In restricted bands, per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -47.2 | -41.2 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Unwanted signal emissions over frequency domain, Conducted measurement, Test Frequency = 915 MHz[2] | $SPUR_{OOB\_FCC}$ | In non-restricted bands, per FCC 47 CFR §15.247[3] | — | -55.0 | -20.0 | dBc |
| | | In restricted bands (30-88 MHz),per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -64.0 | -55.2 | dBm |
| | | In restricted bands (88-216 MHz), per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -65.7 | -51.7 | dBm |
| | | In restricted bands (216-960 MHz), per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -63.0 | -49.2 | dBm |
| | | In restricted bands (>960 MHz), per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -48.2 | -41.2 | dBm |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.
2. The matching network shown in the typical connections section is optimized for best efficiency at 16 dBm. The maximum output power can be above the maximum rating in certain conditions. Emissions are tested at $T_A$ = 25 °C with the output power set to $POUT_{MAX}$.
3. FCC Title 47 CFR Part 15 Section 15.247 Operation within the band 902-928 MHz.
4. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
5. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

#### 4.9.1.2.1 915 MHz Band 0 dBm RF Constant Envelope Transmitter Characteristics

This table is for devices with an output power rating of +16 dBm using the 868/915/920 MHz matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, and DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, crystal frequency = 39.0 MHz, supply filtering as shown in the typical connections section, and RF center frequency 915 MHz.

**Table 4.15. 915 MHz Band 0 dBm RF Constant Envelope Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | 915 | 928 | MHz |
| Establish nominal settings for POUT = 0dBm | $POUT_{0dBm}$ | | — | 0.8 | — | dBm |
| Max Step Size for TX Power setting for POUT between 0 dBm to +12 dBm | $POUT_{STEP}$ | VREGVDD = AVDD = PAVDD = 3.3 V, T = 25 °C | — | 0.1 | — | dB |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR\_V}$ | 3.0 V < VREGVDD = AVDD = PAVDD < 3.8 V, T = 25 °C, and 0 dBm nominal settings | — | 0.03 | 0.08 | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR\_T}$ | $T_A$ = -40 to +85 °C with VREGVDD = AVDD = PAVDD = 3.3 V, and 0 dBm nominal settings | — | 0.7 | 1.8 | dB |
| | | $T_A$ = -40 to +125 °C with VREGVDD = AVDD = PAVDD = 3.3 V, and 0 dBm nominal settings | — | 0.9 | 2.7 | dB |
| Output power variation vs RF frequency | $POUT_{VAR\_F}$ | VREGVDD = AVDD = PAVDD = 3.3 V, and 0 dBm nominal settings, T = 25 °C | — | 0.08 | 0.2 | dB |
| Spurious emissions of harmonics, Conducted measurement, Test Frequency = 915 MHz[1] | $SPUR_{HARM\_FCC}$ | In restricted bands, per FCC 47 CFR §15.205 & §15.209[2] [3], and 0 dBm nominal settings | — | -63.3 | -41.2 | dBm |
| Unwanted signal emissions over frequency domain, Conducted measurement, Test Frequency = 915 MHz[1] | $SPUR_{OOB\_FCC}$ | In restricted bands (30-88 MHz),per FCC 47 CFR §15.205 & §15.209[2] [3], and 0 dBm nominal settings | — | -64.0 | -55.2 | dBm |
| | | In restricted bands (88-216 MHz), per FCC 47 CFR §15.205 & §15.209[2] [3], and 0 dBm nominal settings | — | -65.7 | -51.7 | dBm |
| | | In restricted bands (216-960 MHz), per FCC 47 CFR §15.205 & §15.209[2] [3], and 0 dBm nominal settings | — | -63.0 | -49.2 | dBm |
| | | In restricted bands (>960 MHz), per FCC 47 CFR §15.205 & §15.209[2] [3], and 0 dBm nominal settings | — | -63.1 | -41.2 | dBm |

**Note:**

1. Emissions are tested at $T_A$ = 25 °C.
2. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
3. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

#### 4.9.1.3 868 MHz Band +14 dBm RF Constant Envelope Transmitter Characteristics

This table is for devices with an output power rating of +16 dBm using the 868/915/920 MHz matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, crystal frequency = 39.0 MHz, supply filtering as shown in the typical connections section, and RF center frequency 868.3 MHz.

**Table 4.16. 868 MHz Band +14 dBm RF Constant Envelope Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 863 | — | 870 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | VREGVDD = AVDD = PAVDD = 3.3 V, 16 dBm devices, matching network as shown in the typical connections section[1][2][3] | 13.2 | 14.6 | 15.9 | dBm |
| Minimum active TX power | $POUT_{MIN}$ | | — | -38.4 | — | dBm |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR\_V}$ | 3.0 V < REGVDD = AVDD = PAVDD < 3.8 V, T = 25 °C, and at 14 dBm nominal settings | — | 0.03 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR\_T}$ | $T_A$ = -40 to +85 °C, with REGVDD = AVDD = PAVDD = 3.3 V, and 14 dBm nominal settings | — | 0.8 | 1.3 | dB |
| | | $T_A$ = -40 to +125 °C, with REGVDD = AVDD = PAVDD = 3.3 V, and 14 dBm nominal settings | — | 1.0 | 1.6 | dB |
| Output power variation vs RF frequency | $POUT_{VAR\_F}$ | REGVDD = AVDD = PAVDD = 3.3 V, and 14 dBm nominal settings, T = 25 °C | — | 0.03 | 0.1 | dB |
| Spurious emissions of harmonics, $P_{OUT}$ = +14 dBm, 868.3 MHz[3] | $SPUR_{HARM\_ETSI}$ | (frequencies above 1 GHz)[4] | — | -48.2 | -30.0 | dBm |
| Unwanted emissions in spurious domain, Per ETSI EN 300-220-1[3] [5], $P_{OUT}$ = +14 dBm, 868.3 MHz | $SPUR_{OOB\_ETSI}$ | (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)[4] | — | -68.0 | -54.0 | dBm |
| | | (other frequencies below 1 GHz)[4] | — | -60.5 | -36.0 | dBm |
| | | (frequencies above 1 GHz)[4] | — | -47.4 | -30.0 | dBm |
| Error Vector Magnitude, per IEEE 802.15.4-2020 | EVM | Signal is 100 kbps DSSS O-QPSK reference packet. Modulated according to IEEE 802.15.4-2020 in the 868 MHz band, with pseudo-random packet data content. $P_{OUT}$ = +14 dBm. | — | 6.8 | 35 | % |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.
2. The transmit power for the 863 to 870 Band MHz is normally limited to +14 dBm (25 mW). The 16 dBm devices are recommended for this band with the matching network as shown in the typical connections section.
3. The maximum output power can be above the maximum rating in certain conditions. Emissions for this band are tested at $T_A$ = 25 °C with the output power set to 14 dBm (25 mW) and 0 dBm (1mW).
4. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2
5. Conducted measurement per EN 300-220-1 v3.1.1 5.9.3.3.1

#### 4.9.1.4 470 MHz Band +16 dBm RF Constant Envelope Transmitter Characteristics

This table is for devices with an output power rating of +16 dBm using the 470 MHz Band matching network as shown in the typical connections section. Band is 470 to 510 MHz. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, crystal frequency = 39.0 MHz, supply filtering as shown in the typical connections section, and RF center frequency 490 MHz.

**Table 4.17. 470 MHz Band +16 dBm RF Constant Envelope Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 470 | — | 510 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | PAVDD = 3.3 V, 16 dBm devices | 14.9 | 16.2 | 17.6 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -41.0 | — | dBm |
| Output power variation vs supply, peak to peak | $POUT_{VAR\_V}$ | 3.0 V < REGVDD = AVDD = PAVDD < 3.8 V, T = 25 °C, and at 16 dBm nominal settings | — | 0.04 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR\_T}$ | -40 to +85 °C at 16 dBm nominal settings | — | 0.6 | 1.1 | dB |
| | | -40 to +125 °C at 16 dBm nominal settings | — | 0.7 | 1.5 | dB |
| Output power variation vs RF frequency | $POUT_{VAR\_F}$ | T = 25 °C at 16 dBm nominal settings | — | 0.3 | 0.7 | dB |
| Harmonic emissions, $P_{OUT}$ = +16 dBm, 490 MHz[1] | $SPUR_{HARM\_CN}$ | Per China SRW Requirement, Section 2.1, frequencies below 1GHz | — | -66.2 | -36.0 | dBm |
| | | Per China SRW Requirement, Section 2.1, frequencies above 1GHz | — | -62.0 | -30.0 | dBm |
| Spurious emissions, $P_{OUT}$ = +16 dBm, 490 MHz[1] | $SPUR_{OOB\_CN}$ | Per China SRW Requirement, Section 2.1 (other frequencies below 1GHz) | — | -58.4 | -36.0 | dBm |
| | | Per China SRW Requirement, Section 2.1 (frequencies above 1GHz) | — | -61.4 | -30.0 | dBm |

**Note:**

1. Emissions are tested at $T_A$ = 25 °C.

### 4.9.2 RF SUN OFDM Transmitter Characteristics

OFDM Modulation is defined in IEEE 802.15.4-2020 section 20.3 . In these tables the indication "OptX, MCSy" means X as the Option number 1 through 4, and y is the MCS index 0 through 6, and PL is the Packet PPDU Length in octets. Measurements use packet length of 250 octets when data rate is 50 kbps or higher, and 20 octets packet length when lower than 50 kbps.

#### 4.9.2.1 923 MHz Band RF SUN OFDM Transmitter Characteristics

This table is for devices with an output power rating of +16 dBm using the 920 MHz Band matching network as shown in the typical connections section. $POUT_{13dBm}$[1] is marking the nominal TX setting which is targeting POUT = +13 dBm at typical conditions.

**Table 4.18. 923 MHz Band RF SUN OFDM Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range[2] | $F_{RANGE}$ | | 922.3 | 923.x | 928.1 | MHz |
| Active TX Power for +13 dBm TX output power setting[1] | $POUT_{13dBm}$ | 923.5 MHz, Opt2, MCS3 | — | 13.0 | — | dBm |
| | | 923.5 MHz, Opt2, MCS4 | — | 13.0 | — | dBm |
| | | 923.5 MHz, Opt2, MCS5 | — | 13.1 | — | dBm |
| | | 923.5 MHz, Opt2, MCS6 | — | 13.1 | — | dBm |
| | | 923.7 MHz, Opt3, MCS4[3] | 11.5 | 13.1 | 14.6 | dBm |
| | | 923.7 MHz[4], Opt3, MCS4 | 10.3 | 13.1 | 15.4 | dBm |
| | | 923.7 MHz, Opt3, MCS5 | — | 13.0 | — | dBm |
| | | 923.7 MHz, Opt3, MCS6[3] | 11.6 | 13.1 | 14.6 | dBm |
| | | 923.7 MHz[4], Opt3, MCS6 | 9.1 | 13.1 | 16.1 | dBm |
| | | 923.6 MHz, Opt4, MCS4 | — | 13.0 | — | dBm |
| | | 923.6 MHz, Opt4, MCS5 | — | 13.1 | — | dBm |
| | | 923.6 MHz, Opt4, MCS6 | — | 13.0 | — | dBm |
| Error Vector Magnitude over process variation with TX setting for $POUT_{13dBm}$[1] | $EVM_{13dBm}$ | 923.5 MHz, Opt2, MCS3 | — | -32.2 | — | dB |
| | | 923.5 MHz, Opt2, MCS4 | — | -33.1 | — | dB |
| | | 923.5 MHz, Opt2, MCS5 | — | -32.8 | — | dB |
| | | 923.5 MHz, Opt2, MCS6 | — | -32.5 | — | dB |
| | | 923.7 MHz, Opt3, MCS4[3] | — | -32.8 | -31.0 | dB |
| | | 923.7 MHz[4], Opt3, MCS4 | — | -32.8 | -27.9 | dB |
| | | 923.7 MHz, Opt3, MCS5 | — | -32.4 | — | dB |
| | | 923.7 MHz, Opt3, MCS6[3] | — | -32.8 | -31.0 | dB |
| | | 923.7 MHz[4], Opt3, MCS6 | — | -32.8 | -28.2 | dB |
| | | 923.6 MHz, Opt4, MCS4 | — | -31.5 | — | dB |
| | | 923.6 MHz, Opt4, MCS5 | — | -31.0 | — | dB |
| | | 923.6 MHz, Opt4, MCS6 | — | -32.2 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Error Vector Magnitude in to 2:1 VSWR Load over process variation[5], measured at worst case mis-match phase angle, with TX setting for $POUT_{13dBm}$[1] | $EVM_{VSWR2\_13}$ | 923.5 MHz, Opt2, MCS3, 2:1 VSWR, $T_A$ = 25 °C | — | -27.9 | — | dB |
| | | 923.5 MHz, Opt2, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -28.5 | — | dB |
| | | 923.5 MHz, Opt2, MCS5, 2:1 VSWR, $T_A$ = 25 °C | — | -28.2 | — | dB |
| | | 923.5 MHz, Opt2, MCS6, 2:1 VSWR, $T_A$ = 25 °C | — | -28.1 | — | dB |
| | | 923.7 MHz, Opt3, MCS4, 2:1 VSWR, $T_A$ = 25 °C[3] | — | -28.5 | -27.0 | dB |
| | | 923.7 MHz, Opt3, MCS5, 2:1 VSWR, $T_A$ = 25 °C | — | -28.4 | — | dB |
| | | 923.7 MHz, Opt3, MCS6, 2:1 VSWR, $T_A$ = 25 °C[3] | — | -29.0 | -27.5 | dB |
| | | 923.6 MHz, Opt4, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -29.0 | — | dB |
| | | 923.6 MHz, Opt4, MCS5, 2:1 VSWR, $T_A$ = 25 °C | — | -28.9 | — | dB |
| | | 923.6 MHz, Opt4, MCS6, 2:1 VSWR, $T_A$ = 25 °C | — | -28.7 | — | dB |
| Minimum active TX Power[1] | $POUT_{MIN}$ | 923.5 MHz, Opt2, MCS3 | — | -29.2 | — | dBm |
| | | 923.5 MHz, Opt2, MCS6 | — | -29.1 | — | dBm |
| | | 923.7 MHz, Opt3, MCS4[3] | — | -29.0 | -27.3 | dBm |
| | | 923.7 MHz, Opt3, MCS5 | — | -29.0 | — | dBm |
| | | 923.7 MHz, Opt3, MCS6[3] | — | -28.9 | -27.3 | dBm |
| | | 923.6 MHz, Opt4, MCS4 | — | -29.0 | — | dBm |
| | | 923.6 MHz, Opt4, MCS5 | — | -28.9 | — | dBm |
| | | 923.6 MHz, Opt4, MCS6 | — | -28.9 | — | dBm |
| Output power variation vs PAVDD supply voltage from 3.45 V to 3.8 V with TX setting for $POUT_{13dBm}$ | $PVAR_{V\_13}$ | 923.5 MHz, Opt2, MCS3 | — | 0.1 | — | dB |
| | | 923.5 MHz, Opt2, MCS6 | — | 0.1 | — | dB |
| | | 923.7 MHz, Opt3, MCS4[3] | — | 0.1 | 0.24 | dB |
| | | 923.7 MHz, Opt3, MCS5 | — | 0.1 | — | dB |
| | | 923.7 MHz, Opt3, MCS6[3] | — | 0.1 | 0.20 | dB |
| | | 923.6 MHz, Opt4, MCS4 | — | 0.1 | — | dB |
| | | 923.6 MHz, Opt4, MCS5 | — | 0.1 | — | dB |
| | | 923.6 MHz, Opt4, MCS6 | — | 0.1 | — | dB |
| Active TX Power for +13 dBm TX output power setting at $T_A$ = -40 °C | $POUT_{13\_-40C}$ | 923.7 MHz, Opt3, MCS4 | — | 13.2 | — | dB |
| | | 923.7 MHz, Opt3, MCS6 | — | 12.8 | — | dB |
| Active TX Power for +13 dBm TX output power setting at $T_A$ = 85 °C | $POUT_{13\_85C}$ | 923.7 MHz, Opt3, MCS4 | — | 12.4 | — | dB |
| | | 923.7 MHz, Opt3, MCS6 | — | 12.1 | — | dB |
| Active TX Power for +13 dBm TX output power setting at $T_A$ = 105 °C | $POUT_{13\_105C}$ | 923.7 MHz, Opt3, MCS4 | — | 12.4 | — | dB |
| | | 923.7 MHz, Opt3, MCS6 | — | 11.9 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output power variation vs frequency with TX setting for $POUT_{13dBm}$. Frequency test is at MIN, TYP, and MAX of $F_{RANGE}$ | $PVAR_{F\_13}$ | Opt2, MCS3 | — | 0.1 | — | dB |
| | | Opt2, MCS6 | — | 0.1 | — | dB |
| | | Opt3, MCS4[3] | — | 0.1 | 0.18 | dB |
| | | Opt3, MCS5 | — | 0.1 | — | dB |
| | | Opt3, MCS6[3] | — | 0.1 | 0.18 | dB |
| | | Opt4, MCS4 | — | 0.1 | — | dB |
| | | Opt4, MCS5 | — | 0.1 | — | dB |
| | | Opt4, MCS6 | — | 0.1 | — | dB |
| Spurious emission at $f_{SPUR}$ below 710 MHz, while on channel desired signal is at POUT = +13 dBm, conducted measurement with 100 kHz RBW[6] [7] | $SPUR_{ARIBL}$ | 923.5 MHz, Opt2, MCS3 | — | -59.8 | -36 | dBm |
| | | 923.5 MHz, Opt2, MCS6 | — | -60.4 | -36 | dBm |
| | | 923.7 MHz, Opt3, MCS4 | — | -59.7 | -36 | dBm |
| | | 923.7 MHz, Opt3, MCS5 | — | -60.2 | -36 | dBm |
| | | 923.7 MHz, Opt3, MCS6 | — | -60.3 | -36 | dBm |
| | | 923.6 MHz, Opt4, MCS4 | — | -60.4 | -36 | dBm |
| | | 923.6 MHz, Opt4, MCS5 | — | -60.4 | -36 | dBm |
| | | 923.6 MHz, Opt4, MCS6 | — | -60.5 | -36 | dBm |
| Spurious emission at 710 MHz < $f_{SPUR}$ ≤ 900 MHz, while on channel desired signal is at POUT = +13 dBm, conducted measurement with 1 MHz RBW[6] [7] | $SPUR_{ARIB710}$ | 923.5 MHz, Opt2, MCS3[8] | — | -60.7 | -55 | dB |
| | | 923.5 MHz, Opt2, MCS6[8] | — | -61.5 | -55 | dB |
| | | 923.7 MHz, Opt3, MCS4[8] | — | -61.1 | -55 | dB |
| | | 923.7 MHz, Opt3, MCS5[8] | — | -61.6 | -55 | dB |
| | | 923.7 MHz, Opt3, MCS6[8] | — | -61.2 | -55 | dB |
| | | 923.6 MHz, Opt4, MCS4[8] | — | -61.0 | -55 | dB |
| | | 923.6 MHz, Opt4, MCS5[8] | — | -60.8 | -55 | dB |
| | | 923.6 MHz, Opt4, MCS6[8] | — | -60.7 | -55 | dB |
| Spurious emission at 900 MHz < $f_{SPUR}$ ≤ 915 MHz, while on channel desired signal is at POUT = +13 dBm, conducted measurement with 100 kHz RBW[6] [7] | $SPUR_{ARIB900}$ | 923.5 MHz, Opt2, MCS3[8] | — | -68.4 | -55 | dBm |
| | | 923.5 MHz, Opt2, MCS6[8] | — | -69.5 | -55 | dBm |
| | | 923.7 MHz, Opt3, MCS4[8] | — | -68.9 | -55 | dBm |
| | | 923.7 MHz, Opt3, MCS5[8] | — | -70.0 | -55 | dBm |
| | | 923.7 MHz, Opt3, MCS6[8] | — | -68.8 | -55 | dBm |
| | | 923.6 MHz, Opt4, MCS4[8] | — | -69.8 | -55 | dBm |
| | | 923.6 MHz, Opt4, MCS5[8] | — | -68.9 | -55 | dBm |
| | | 923.6 MHz, Opt4, MCS6[8] | — | -69.0 | -55 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious emission at 915 MHz < $f_{SPUR}$ ≤ 930 MHz except within 200 kHz of occupied channel which is an integer number of 200 kHz wide radio channel units, while on channel desired signal is at POUT = +13 dBm, conducted measurement with 100 kHz RBW, and ARIB STD-T108 part 2, section 3.2.8 and sections 3.2.7 (3) and (4)[7] | $SPUR_{ARIB915}$ | 923.5 MHz, Opt2, MCS3[9] | — | -37.3 | -36 | dB |
| | | 923.5 MHz, Opt2, MCS6[9] | — | -38.2 | -36 | dB |
| | | 923.7 MHz, Opt3, MCS4[9] | — | -47.3 | -36 | dB |
| | | 923.7 MHz, Opt3, MCS5[9] | — | -46.8 | -36 | dB |
| | | 923.7 MHz, Opt3, MCS6[9] | — | -46.6 | -36 | dB |
| | | 923.6 MHz, Opt4, MCS4[9] | — | -44.6 | -36 | dB |
| | | 923.6 MHz, Opt4, MCS5[9] | — | -44.9 | -36 | dB |
| | | 923.6 MHz, Opt4, MCS6[9] | — | -45.3 | -36 | dB |
| Spurious emission at 930 MHz < $f_{SPUR}$ ≤ 1000 MHz, while on channel desired signal is at POUT = +13 dBm, conducted measurement with 100 kHz RBW[6] [7] | $SPUR_{ARIB930}$ | 923.5 MHz, Opt2, MCS3[8] | — | -67.5 | -55 | dBm |
| | | 923.5 MHz, Opt2, MCS6[8] | — | -67.7 | -55 | dBm |
| | | 923.7 MHz, Opt3, MCS4[8] | — | -67.5 | -55 | dBm |
| | | 923.7 MHz, Opt3, MCS5[8] | — | -68.6 | -55 | dBm |
| | | 923.7 MHz, Opt3, MCS6[8] | — | -67.3 | -55 | dBm |
| | | 927.9 MHz, Opt3, MCS4[8] | — | -58.0 | -55 | dBm |
| | | 927.9 MHz, Opt3, MCS5[8] | — | -63.3 | -55 | dBm |
| | | 927.9 MHz, Opt3, MCS6[8] | — | -60.0 | -55 | dBm |
| | | 923.6 MHz, Opt4, MCS4[8] | — | -67.0 | -55 | dBm |
| | | 923.6 MHz, Opt4, MCS5[8] | — | -67.5 | -55 | dBm |
| | | 923.6 MHz, Opt4, MCS6[8] | — | -67.5 | -55 | dBm |
| Spurious emission at 1000 MHz < $f_{SPUR}$ ≤ 1215 MHz, while on channel desired signal is at POUT = +13 dBm, conducted measurement with 1 MHz RBW[6] [7] | $SPUR_{ARIB1000}$ | 923.5 MHz, Opt2, MCS3 | — | -49.1 | -45 | dB |
| | | 923.5 MHz, Opt2, MCS6 | — | -48.6 | -45 | dB |
| | | 923.7 MHz, Opt3, MCS4 | — | -48.9 | -45 | dB |
| | | 923.7 MHz, Opt3, MCS5 | — | -48.6 | -45 | dB |
| | | 923.7 MHz, Opt3, MCS6 | — | -48.9 | -45 | dB |
| | | 923.6 MHz, Opt4, MCS4 | — | -48.9 | -45 | dB |
| | | 923.6 MHz, Opt4, MCS5 | — | -48.5 | -45 | dB |
| | | 923.6 MHz, Opt4, MCS6 | — | -48.7 | -45 | dB |
| Spurious emission at 1215 MHz < $f_{SPUR}$, while on channel desired signal is at POUT = +13 dBm, conducted measurement with 1 MHz RBW[6] [7] | $SPUR_{ARIB1215}$ | 923.5 MHz, Opt2, MCS3 | — | -46.7 | -30 | dBm |
| | | 923.5 MHz, Opt2, MCS6 | — | -46.6 | -30 | dBm |
| | | 923.7 MHz, Opt3, MCS4 | — | -51.4 | -30 | dBm |
| | | 923.7 MHz, Opt3, MCS5 | — | -49.7 | -30 | dBm |
| | | 923.7 MHz, Opt3, MCS6 | — | -48.9 | -30 | dBm |
| | | 923.6 MHz, Opt4, MCS4 | — | -47.4 | -30 | dBm |
| | | 923.6 MHz, Opt4, MCS5 | — | -49.4 | -30 | dBm |
| | | 923.6 MHz, Opt4, MCS6 | — | -49.0 | -30 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Adjacent Channel Leakage Power while on channel desired signal is at POUT = +13 dBm, conducted measurement integrating power from the channel edge outward 200 kHz, and ARIB STD-T108 part 2, section 3.2.7 (4)[7] | $ACLP_{ARIB\_13dBm}$ | 923.5 MHz, Opt2, MCS3 | — | -20.9 | -15 | dBm |
| | | 923.5 MHz, Opt2, MCS4 | — | -20.6 | -15 | dBm |
| | | 923.5 MHz, Opt2, MCS5 | — | -20.6 | -15 | dBm |
| | | 923.5 MHz, Opt2, MCS6 | — | -21.4 | -15 | dBm |
| | | 923.7 MHz, Opt3, MCS4 | — | -19.8 | -15 | dBm |
| | | 923.7 MHz, Opt3, MCS5 | — | -19.8 | -15 | dBm |
| | | 923.7 MHz, Opt3, MCS6 | — | -19.8 | -15 | dBm |
| | | 923.6 MHz, Opt4, MCS4 | — | -17.9 | -15 | dBm |
| | | 923.6 MHz, Opt4, MCS5 | — | -18.2 | -15 | dBm |
| | | 923.6 MHz, Opt4, MCS6 | — | -18.2 | -15 | dBm |
| Adjacent Channel Leakage Power while on channel desired signal is at POUT = 0 dBm, conducted measurement integrating power from the channel edge outward 200 kHz, and ARIB STD-T108 part 2, section 3.2.7 (3)[7] | $ACLP_{ARIB\_0dBm}$ | 923.5 MHz, Opt2, MCS3 | — | -45.6 | -26 | dBm |
| | | 923.5 MHz, Opt2, MCS4 | — | -45.5 | -26 | dBm |
| | | 923.5 MHz, Opt2, MCS5 | — | -45.4 | -26 | dBm |
| | | 923.5 MHz, Opt2, MCS6 | — | -45.5 | -26 | dBm |
| | | 923.7 MHz, Opt3, MCS4 | — | -42.9 | -26 | dBm |
| | | 923.7 MHz, Opt3, MCS5 | — | -42.9 | -26 | dBm |
| | | 923.7 MHz, Opt3, MCS6 | — | -42.8 | -26 | dBm |
| | | 923.6 MHz, Opt4, MCS4 | — | -40.5 | -26 | dBm |
| | | 923.6 MHz, Opt4, MCS5 | — | -40.6 | -26 | dBm |
| | | 923.6 MHz, Opt4, MCS6 | — | -40.6 | -26 | dBm |
| Adjacent Channel Power Ratio while on channel desired signal is at POUT = +13 dBm per Wi-SUN Alliance[7] [10] | $ACPR_{WISUN}$ | 923.5 MHz, Opt2, MCS3 | 20 | 31.9 | — | dBc |
| | | 923.5 MHz, Opt2, MCS4 | 20 | 32.2 | — | dBc |
| | | 923.5 MHz, Opt2, MCS5 | 20 | 32.1 | — | dBc |
| | | 923.5 MHz, Opt2, MCS6 | 20 | 32.4 | — | dBc |
| | | 923.7 MHz, Opt3, MCS4 | 20 | 31.8 | — | dBc |
| | | 923.7 MHz, Opt3, MCS5 | 20 | 31.7 | — | dBc |
| | | 923.7 MHz, Opt3, MCS6 | 20 | 31.6 | — | dBc |
| | | 923.6 MHz, Opt4, MCS4 | 20 | 30.5 | — | dBc |
| | | 923.6 MHz, Opt4, MCS5 | 20 | 30.6 | — | dBc |
| | | 923.6 MHz, Opt4, MCS6 | 20 | 30.7 | — | dBc |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Alternate Adjacent Channel Power Ratio while on channel desired signal is at POUT = +13 dBm per Wi-SUN Alliance[7] [10] | $A2CPR_{WISUN}$ | 923.5 MHz, Opt2, MCS3 | 40 | 48.5 | — | dBc |
| | | 923.5 MHz, Opt2, MCS4 | 40 | 48.4 | — | dBc |
| | | 923.5 MHz, Opt2, MCS5 | 40 | 48.5 | — | dBc |
| | | 923.5 MHz, Opt2, MCS6 | 40 | 48.4 | — | dBc |
| | | 923.7 MHz, Opt3, MCS4 | 40 | 48.8 | — | dBc |
| | | 923.7 MHz, Opt3, MCS5 | 40 | 48.8 | — | dBc |
| | | 923.7 MHz, Opt3, MCS6 | 40 | 48.8 | — | dBc |
| | | 923.6 MHz, Opt4, MCS4 | 40 | 46.4 | — | dBc |
| | | 923.6 MHz, Opt4, MCS5 | 40 | 46.3 | — | dBc |
| | | 923.6 MHz, Opt4, MCS6 | 40 | 46.4 | — | dBc |

**Note:**

1. With compliance to ARIB STD-T108 part 2, Wi-SUN Alliance PHY Working Group Technical Specification Revision 1VA9, and IEEE 802.15.4-2020 Section 20 except for max power limit
2. Typical frequency is defined in the Test Condition column, and varies on selected Option.
3. Min/Max numbers are measured at typical voltage, at typical $F_{RANGE}$ frequency, and at $T_A$ = 25 °C.
4. Frequency value used for typical measurements
5. Other operating conditions are kept at Typical values.
6. Per ARIB STD-T108 part 2, section 3.2.8
7. Emissions are measured at $T_A$ = 25 °C
8. The spurious emission is calculated according to TELEC-T245 5th Ed. Spurious Emissions Measurement Procedure Section 4 (1) to (4).
9. The spurious emission is calculated according to TELEC-T245 5th Ed. Spurious Emissions Measurement Procedure Section 4 (6) to (16).
10. All Operating Conditions are Typical / Nominal only in accordance to Wi-SUN Alliance PHY Working Group Technical Specification Revision 1VA9 section 8.2.7.

#### 4.9.2.2 914 MHz Band RF SUN OFDM Transmitter Characteristics

This table is for devices with an output power rating of +16 dBm using the 915 MHz Band matching network as shown in the typical connections section. $POUT_{16dBm}$[1] is marking the nominal TX setting which is targeting +16 dBm output power at typical conditions. $POUT_{12dBm}$[1] is marking the nominal TX setting which is targeting +12 dBm output power at typical conditions.

**Table 4.19. 914 MHz Band RF SUN OFDM Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | 914 | 928 | MHz |
| Active TX Power for +16 dBm TX output power setting[1] | $POUT_{16dBm}$ | Opt1, MCS2[2] | 14.8 | 16.1 | 17.3 | dBm |
| | | Opt1, MCS2 | 14.1 | 16.1 | 18.2 | dBm |
| | | Opt1, MCS3 | — | 16.1 | — | dBm |
| | | Opt1, MCS4 | — | 16.0 | — | dBm |
| | | Opt1, MCS5 | — | 16.0 | — | dBm |
| | | Opt1, MCS6[2] | 14.7 | 16.0 | 17.3 | dBm |
| | | Opt1, MCS6 | 14.1 | 16.0 | 17.4 | dBm |
| | | Opt2, MCS3[2] | 14.8 | 16.1 | 17.3 | dBm |
| | | Opt2, MCS3 | 14.2 | 16.1 | 17.5 | dBm |
| | | Opt2, MCS4 | — | 16.0 | — | dBm |
| | | Opt2, MCS5 | — | 16.1 | — | dBm |
| | | Opt2, MCS6[2] | 14.8 | 16.0 | 17.2 | dBm |
| | | Opt2, MCS6 | 12.6 | 16.0 | 19.2 | dBm |
| | | Opt3, MCS4 | — | 16.0 | — | dBm |
| | | Opt3, MCS6 | — | 16.1 | — | dBm |
| Error Vector Magnitude over process variation with TX setting for $POUT_{16dBm}$[1] | $EVM_{16dBm}$ | Opt1, MCS2 | — | -25.4 | — | dB |
| | | Opt1, MCS3 | — | -26.1 | — | dB |
| | | Opt1, MCS4 | — | -25.9 | — | dB |
| | | Opt1, MCS5 | — | -26.5 | — | dB |
| | | Opt1, MCS6 | — | -26.4 | — | dB |
| | | Opt2, MCS3 | — | -25.5 | — | dB |
| | | Opt2, MCS4 | — | -26.3 | — | dB |
| | | Opt2, MCS5 | — | -26.4 | — | dB |
| | | Opt2, MCS6 | — | -25.7 | — | dB |
| | | Opt3, MCS4 | — | -26.0 | — | dB |
| | | Opt3, MCS6 | — | -26.5 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Error Vector Magnitude in to 2:1 VSWR Load over process variation[3], measured at worst case mis-match phase angle, with TX settings for $POUT_{16dBm}$[1] | $EVM_{VSWR2\_16}$ | Opt1, MCS2, 2:1 VSWR, $T_A$ = 25 °C[2] | — | -20.7 | -19.2 | dB |
| | | Opt1, MCS3, 2:1 VSWR, $T_A$ = 25 °C | — | -21.0 | — | dB |
| | | Opt1, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -21.1 | — | dB |
| | | Opt1, MCS5, 2:1 VSWR, $T_A$ = 25 °C | — | -21.2 | — | dB |
| | | Opt1, MCS6, 2:1 VSWR, $T_A$ = 25 °C[2] | — | -21.3 | -19.5 | dB |
| | | Opt2, MCS3, 2:1 VSWR, $T_A$ = 25 °C[2] | — | -21.4 | -19.5 | dB |
| | | Opt2, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -21.6 | — | dB |
| | | Opt2, MCS5, 2:1 VSWR, $T_A$ = 25 °C | — | -21.7 | — | dB |
| | | Opt2, MCS6, 2:1 VSWR, $T_A$ = 25 °C[2] | — | -21.6 | -20.0 | dB |
| | | Opt3, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -21.9 | — | dB |
| | | Opt3, MCS6, 2:1 VSWR, $T_A$ = 25 °C | — | -22.0 | — | dB |
| Output power variation vs PAVDD supply voltage from 3.45 V to 3.8 V with TX setting for $POUT_{16dBm}$ | $PVAR_{V\_16}$ | Opt1, MCS2[2] | — | 0.1 | 0.25 | dB |
| | | Opt1, MCS3 | — | 0.1 | — | dB |
| | | Opt1, MCS4 | — | 0.1 | — | dB |
| | | Opt1, MCS5 | — | 0.1 | — | dB |
| | | Opt1, MCS6[2] | — | 0.1 | 0.45 | dB |
| | | Opt2, MCS3[2] | — | 0.1 | 0.27 | dB |
| | | Opt2, MCS4 | — | 0.1 | — | dB |
| | | Opt2, MCS5 | — | 0.1 | — | dB |
| | | Opt2, MCS6[2] | — | 0.1 | 0.26 | dB |
| | | Opt3, MCS4 | — | 0.1 | — | dB |
| | | Opt3, MCS6 | — | 0.1 | — | dB |
| Active TX Power for +16 dBm TX output power setting at $T_A$ = -40 °C | $POUT_{16\_-40C}$ | Opt1, MCS2[4] | — | 16.1 | — | dBm |
| | | Opt1, MCS6[4] | — | 16.2 | — | dBm |
| | | Opt2, MCS3[4] | — | 16.2 | — | dBm |
| | | Opt2, MCS6[4] | — | 16.0 | — | dBm |
| Active TX Power for +16 dBm TX output power setting at $T_A$ = 85 °C | $POUT_{16\_85C}$ | Opt1, MCS2[4] | — | 15.6 | — | dBm |
| | | Opt1, MCS6[4] | — | 15.7 | — | dBm |
| | | Opt2, MCS3[4] | — | 15.7 | — | dBm |
| | | Opt2, MCS6[4] | — | 15.5 | — | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active TX Power for +16 dBm TX output power setting at $T_A$ = 105 °C | $POUT_{16\_105C}$ | Opt1, MCS2[4] | — | 15.5 | — | dBm |
| | | Opt1, MCS6[4] | — | 15.5 | — | dBm |
| | | Opt2, MCS3[4] | — | 15.6 | — | dBm |
| | | Opt2, MCS6[4] | — | 15.4 | — | dBm |
| Output power variation vs frequency with TX setting for $POUT_{16dBm}$. Frequency test is at MIN, TYP, and MAX of $F_{RANGE}$ | $PVAR_{F\_16}$ | Opt1, MCS2[2] | — | 0.15 | 0.39 | dB |
| | | Opt1, MCS3 | — | 0.15 | — | dB |
| | | Opt1, MCS4 | — | 0.15 | — | dB |
| | | Opt1, MCS5 | — | 0.15 | — | dB |
| | | Opt1, MCS6[2] | — | 0.15 | 0.43 | dB |
| | | Opt2, MCS3[2] | — | 0.15 | 0.38 | dB |
| | | Opt2, MCS4 | — | 0.15 | — | dB |
| | | Opt2, MCS5 | — | 0.15 | — | dB |
| | | Opt2, MCS6[2] | — | 0.15 | 0.38 | dB |
| | | Opt3, MCS4 | — | 0.15 | — | dB |
| | | Opt3, MCS6 | — | 0.15 | — | dB |
| Active TX Power for +12 dBm TX output power setting[1] | $POUT_{12dBm}$ | Opt1, MCS2[2] | 10.7 | 12.1 | 13.3 | dBm |
| | | Opt1, MCS2 | 9.1 | 12.1 | 14.5 | dBm |
| | | Opt1, MCS3 | — | 12.1 | — | dBm |
| | | Opt1, MCS4 | — | 12.1 | — | dBm |
| | | Opt1, MCS5 | — | 12.1 | — | dBm |
| | | Opt1, MCS6[2] | 10.6 | 12.1 | 13.3 | dBm |
| | | Opt1, MCS6 | 7.3 | 12.1 | 16.3 | dBm |
| | | Opt2, MCS3[2] | 10.6 | 12.0 | 13.2 | dBm |
| | | Opt2, MCS3 | 9.5 | 12.0 | 14.3 | dBm |
| | | Opt2, MCS4 | — | 12.1 | — | dBm |
| | | Opt2, MCS5 | — | 12.1 | — | dBm |
| | | Opt2, MCS6[2] | 10.6 | 12.1 | 13.2 | dBm |
| | | Opt2, MCS6 | 7.5 | 12.1 | 15.2 | dBm |
| | | Opt3, MCS4 | — | 12.1 | — | dBm |
| | | Opt3, MCS6 | — | 12.1 | — | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Error Vector Magnitude over process variation with TX setting for $POUT_{12dBm}$[1] | $EVM_{12dBm}$ | Opt1, MCS2 | — | -34.2 | — | dB |
| | | Opt1, MCS3 | — | -34.7 | — | dB |
| | | Opt1, MCS4 | — | -34.1 | — | dB |
| | | Opt1, MCS5 | — | -34.3 | — | dB |
| | | Opt1, MCS6 | — | -34.6 | — | dB |
| | | Opt2, MCS3 | — | -34.3 | — | dB |
| | | Opt2, MCS4 | — | -34.6 | — | dB |
| | | Opt2, MCS5 | — | -34.6 | — | dB |
| | | Opt2, MCS6 | — | -34.1 | — | dB |
| | | Opt3, MCS4 | — | -34.0 | — | dB |
| | | Opt3, MCS6 | — | -34.4 | — | dB |
| Error Vector Magnitude in to 2:1 VSWR Load over process variation[3], measured at worst case mis-match phase angle, with TX settings for $POUT_{12dBm}$[1] | $EVM_{VSWR2\_12}$ | Opt1, MCS2, 2:1 VSWR, $T_A$ = 25 °C[2] | — | -31.1 | -28.0 | dB |
| | | Opt1, MCS3, 2:1 VSWR, $T_A$ = 25 °C | — | -30.6 | — | dB |
| | | Opt1, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -30.1 | — | dB |
| | | Opt1, MCS5, 2:1 VSWR, $T_A$ = 25 °C | — | -30.5 | — | dB |
| | | Opt1, MCS6, 2:1 VSWR, $T_A$ = 25 °C[2] | — | -30.6 | -28.3 | dB |
| | | Opt2, MCS3, 2:1 VSWR, $T_A$ = 25 °C[2] | — | -30.2 | -28.7 | dB |
| | | Opt2, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -29.8 | — | dB |
| | | Opt2, MCS5, 2:1 VSWR, $T_A$ = 25 °C | — | -30.7 | — | dB |
| | | Opt2, MCS6, 2:1 VSWR, $T_A$ = 25 °C[2] | — | -29.7 | -28.6 | dB |
| | | Opt3, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -30.2 | — | dB |
| | | Opt3, MCS6, 2:1 VSWR, $T_A$ = 25 °C | — | -29.5 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output power variation vs PAVDD supply voltage from 3.45 V to 3.8 V with TX setting for $POUT_{12dBm}$ | $PVAR_{V\_12}$ | Opt1, MCS2[2] | — | 0.1 | 0.17 | dB |
| | | Opt1, MCS3 | — | 0.1 | — | dB |
| | | Opt1, MCS4 | — | 0.1 | — | dB |
| | | Opt1, MCS5 | — | 0.1 | — | dB |
| | | Opt1, MCS6[2] | — | 0.1 | 0.23 | dB |
| | | Opt2, MCS3[2] | — | 0.1 | 0.17 | dB |
| | | Opt2, MCS4 | — | 0.1 | — | dB |
| | | Opt2, MCS5 | — | 0.1 | — | dB |
| | | Opt2, MCS6[2] | — | 0.1 | 0.14 | dB |
| | | Opt3, MCS4 | — | 0.1 | — | dB |
| | | Opt3, MCS6 | — | 0.1 | — | dB |
| Active TX Power for +12 dBm TX output power setting at $T_A$ = -40 °C | $POUT_{12\_-40C}$ | Opt1, MCS2[4] | — | 12.0 | — | dBm |
| | | Opt1, MCS6[4] | — | 12.1 | — | dBm |
| | | Opt2, MCS3[4] | — | 12.1 | — | dBm |
| | | Opt2, MCS6[4] | — | 12.0 | — | dBm |
| Active TX Power for +12 dBm TX output power setting at $T_A$ = 85 °C | $POUT_{12\_85C}$ | Opt1, MCS2[4] | — | 11.4 | — | dBm |
| | | Opt1, MCS6[4] | — | 11.7 | — | dBm |
| | | Opt2, MCS3[4] | — | 11.5 | — | dBm |
| | | Opt2, MCS6[4] | — | 11.2 | — | dBm |
| Active TX Power for +12 dBm TX output power setting at $T_A$ = 105 °C | $POUT_{12\_105C}$ | Opt1, MCS2[4] | — | 11.2 | — | dBm |
| | | Opt1, MCS6[4] | — | 11.4 | — | dBm |
| | | Opt2, MCS3[4] | — | 11.3 | — | dBm |
| | | Opt2, MCS6[4] | — | 11.0 | — | dBm |
| Output power variation vs frequency with TX setting for $POUT_{12dBm}$. Frequency test is at MIN, TYP, and MAX of $F_{RANGE}$ | $PVAR_{F\_12}$ | Opt1, MCS2[2] | — | 0.1 | 0.32 | dB |
| | | Opt1, MCS3 | — | 0.1 | — | dB |
| | | Opt1, MCS4 | — | 0.1 | — | dB |
| | | Opt1, MCS5 | — | 0.1 | — | dB |
| | | Opt1, MCS6[2] | — | 0.1 | 0.50 | dB |
| | | Opt2, MCS3[2] | — | 0.1 | 0.31 | dB |
| | | Opt2, MCS4 | — | 0.1 | — | dB |
| | | Opt2, MCS5 | — | 0.1 | — | dB |
| | | Opt2, MCS6[2] | — | 0.1 | 0.34 | dB |
| | | Opt3, MCS4 | — | 0.1 | — | dB |
| | | Opt3, MCS6 | — | 0.1 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Minimum active TX Power, PAVDD is Minimum of 3.45 V, and Typical of 3.6 V, and max of 3.8 V[1] | $POUT_{MIN}$ | Opt1, MCS2[2] | — | -29.1 | -27.6 | dBm |
| | | Opt1, MCS3 | — | -28.9 | — | dBm |
| | | Opt1, MCS4 | — | -28.9 | — | dBm |
| | | Opt1, MCS5 | — | -28.8 | — | dBm |
| | | Opt1, MCS6[2] | — | -28.7 | -27.2 | dBm |
| | | Opt2, MCS3[2] | — | -29.3 | -27.7 | dBm |
| | | Opt2, MCS4 | — | -29.2 | — | dBm |
| | | Opt2, MCS5 | — | -29.2 | — | dBm |
| | | Opt2, MCS6[2] | — | -29.2 | -27.7 | dBm |
| | | Opt3, MCS4 | — | -29.0 | — | dBm |
| | | Opt3, MCS6 | — | -29.1 | — | dBm |
| Max Step Size for TX Power setting for POUT between 0 dBm to +12 dBm | $POUT_{STEP}$ | VREGVDD = AVDD = PAVDD = 3.6 V, T = 25 °C | — | 0.1 | — | dB |
| Spurious emissions of harmonics in non-restricted bands using average power detector, per FCC 47 CFR Part 15.247 with TX setting for $POUT_{16dBm}$[5 6] | $HARM_{FCCNR}$ | Opt1, MCS2 | — | -68.7 | -20 | dBc |
| | | Opt1, MCS3 | — | -67.7 | -20 | dBc |
| | | Opt1, MCS4 | — | -68.4 | -20 | dBc |
| | | Opt1, MCS5 | — | -69.0 | -20 | dBc |
| | | Opt1, MCS6 | — | -67.9 | -20 | dBc |
| | | Opt2, MCS3 | — | -65.5 | -20 | dBc |
| | | Opt2, MCS4 | — | -64.8 | -20 | dBc |
| | | Opt2, MCS5 | — | -66.4 | -20 | dBc |
| | | Opt2, MCS6 | — | -66.2 | -20 | dBc |
| | | Opt3, MCS4 | — | -63.3 | -20 | dBc |
| | | Opt3, MCS6 | — | -63.2 | -20 | dBc |
| Spurious emissions of harmonics in restricted bands using average power detector, per FCC 47 CFR Part 15.247, Part 15.205, and Part 15.209 with TX setting for $POUT_{16dBm}$[5 6] | $HARM_{FCCRS}$ | Opt1, MCS2 | — | -59.0 | -41.2 | dBm |
| | | Opt1, MCS3 | — | -59.2 | -41.2 | dBm |
| | | Opt1, MCS4 | — | -58.8 | -41.2 | dBm |
| | | Opt1, MCS5 | — | -59.0 | -41.2 | dBm |
| | | Opt1, MCS6 | — | -59.7 | -41.2 | dBm |
| | | Opt2, MCS3 | — | -57.6 | -41.2 | dBm |
| | | Opt2, MCS4 | — | -57.0 | -41.2 | dBm |
| | | Opt2, MCS5 | — | -57.5 | -41.2 | dBm |
| | | Opt2, MCS6 | — | -57.5 | -41.2 | dBm |
| | | Opt3, MCS4 | — | -56.5 | -41.2 | dBm |
| | | Opt3, MCS6 | — | -55.0 | -41.2 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious emissions out-of-band, in non-restricted bands per FCC 47 CFR Part 15.247 with TX setting for $POUT_{16dBm}$[6] | $OOB_{FCCNR}$ | Opt1, MCS2 | — | -41.0 | -20 | dBc |
| | | Opt1, MCS3 | — | -34.9 | -20 | dBc |
| | | Opt1, MCS4 | — | -34.5 | -20 | dBc |
| | | Opt1, MCS5 | — | -38.0 | -20 | dBc |
| | | Opt1, MCS6 | — | -39.4 | -20 | dBc |
| | | Opt2, MCS3 | — | -38.9 | -20 | dBc |
| | | Opt2, MCS4 | — | -31.9 | -20 | dBc |
| | | Opt2, MCS5 | — | -31.6 | -20 | dBc |
| | | Opt2, MCS6 | — | -43.3 | -20 | dBc |
| | | Opt3, MCS4 | — | -53.7 | -20 | dBc |
| | | Opt3, MCS6 | — | -57.1 | -20 | dBc |
| Spurious emissions out-of-band, in restricted bands (30-88 MHz) per FCC 47 CFR Part 15.247, Part 15.205, and Part 15.209 with TX setting for $POUT_{16dBm}$[6] | $OOB_{FCC30}$ | Opt1, MCS2 | — | -59.7 | -41.2 | dBm |
| | | Opt1, MCS3 | — | -59.9 | -41.2 | dBm |
| | | Opt1, MCS4 | — | -59.9 | -41.2 | dBm |
| | | Opt1, MCS5 | — | -60.0 | -41.2 | dBm |
| | | Opt1, MCS6 | — | -60.0 | -41.2 | dBm |
| | | Opt2, MCS3 | — | -60.0 | -41.2 | dBm |
| | | Opt2, MCS4 | — | -59.7 | -41.2 | dBm |
| | | Opt2, MCS5 | — | -59.9 | -41.2 | dBm |
| | | Opt2, MCS6 | — | -59.9 | -41.2 | dBm |
| | | Opt3, MCS4 | — | -59.9 | -41.2 | dBm |
| | | Opt3, MCS6 | — | -59.9 | -41.2 | dBm |
| Spurious emissions out-of-band, in restricted bands (88-216 MHz) per FCC 47 CFR Part 15.247, Part 15.205, and Part 15.209 with TX setting for $POUT_{16dBm}$[6] | $OOB_{FCC88}$ | Opt1, MCS2 | — | -61.1 | -41.2 | dBm |
| | | Opt1, MCS3 | — | -61.1 | -41.2 | dBm |
| | | Opt1, MCS4 | — | -61.0 | -41.2 | dBm |
| | | Opt1, MCS5 | — | -61.2 | -41.2 | dBm |
| | | Opt1, MCS6 | — | -61.5 | -41.2 | dBm |
| | | Opt2, MCS3 | — | -61.2 | -41.2 | dBm |
| | | Opt2, MCS4 | — | -61.5 | -41.2 | dBm |
| | | Opt2, MCS5 | — | -61.4 | -41.2 | dBm |
| | | Opt2, MCS6 | — | -61.4 | -41.2 | dBm |
| | | Opt3, MCS4 | — | -61.4 | -41.2 | dBm |
| | | Opt3, MCS6 | — | -61.3 | -41.2 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious emissions out-of-band, in restricted bands (216-960 MHz) per FCC 47 CFR Part 15.247, Part 15.205, and Part 15.209 with TX setting for $POUT_{16dBm}$[6] | $OOB_{FCC216}$ | Opt1, MCS2 | — | -61.6 | -41.2 | dBm |
| | | Opt1, MCS3 | — | -60.6 | -41.2 | dBm |
| | | Opt1, MCS4 | — | -60.6 | -41.2 | dBm |
| | | Opt1, MCS5 | — | -60.7 | -41.2 | dBm |
| | | Opt1, MCS6 | — | -60.6 | -41.2 | dBm |
| | | Opt2, MCS3 | — | -60.8 | -41.2 | dBm |
| | | Opt2, MCS4 | — | -60.8 | -41.2 | dBm |
| | | Opt2, MCS5 | — | -60.7 | -41.2 | dBm |
| | | Opt2, MCS6 | — | -60.8 | -41.2 | dBm |
| | | Opt3, MCS4 | — | -60.8 | -41.2 | dBm |
| | | Opt3, MCS6 | — | -60.8 | -41.2 | dBm |
| Spurious emissions out-of-band, in restricted bands (>960 MHz) per FCC 47 CFR Part 15.247, Part 15.205, and Part 15.209 with TX setting for $POUT_{16dBm}$[6] | $OOB_{FCC960}$ | Opt1, MCS2 | — | -57.5 | -41.2 | dBm |
| | | Opt1, MCS3 | — | -57.3 | -41.2 | dBm |
| | | Opt1, MCS4 | — | -57.0 | -41.2 | dBm |
| | | Opt1, MCS5 | — | -57.4 | -41.2 | dBm |
| | | Opt1, MCS6 | — | -58.0 | -41.2 | dBm |
| | | Opt2, MCS3 | — | -57.1 | -41.2 | dBm |
| | | Opt2, MCS4 | — | -57.6 | -41.2 | dBm |
| | | Opt2, MCS5 | — | -57.6 | -41.2 | dBm |
| | | Opt2, MCS6 | — | -57.5 | -41.2 | dBm |
| | | Opt3, MCS4 | — | -57.3 | -41.2 | dBm |
| | | Opt3, MCS6 | — | -57.4 | -41.2 | dBm |
| Power Spectral Density (Average method per ANSI C63. 10-2020 11.10.3 AVGPSD-1) at frequency of highest level for a 3 kHz window with TX setting for $POUT_{16dBm}$[1 6] | $PSD_{3kHz\_16}$ | Opt1, MCS2 | — | -3.9 | — | dBm/ 3kHz |
| | | Opt1, MCS3 | — | -3.1 | — | dBm/ 3kHz |
| | | Opt1, MCS4 | — | -2.7 | — | dBm/ 3kHz |
| | | Opt1, MCS5 | — | -2.6 | — | dBm/ 3kHz |
| | | Opt1, MCS6 | — | -2.5 | — | dBm/ 3kHz |
| | | Opt2, MCS3 | — | -2.7 | — | dBm/ 3kHz |
| | | Opt2, MCS4 | — | -2.5 | — | dBm/ 3kHz |
| | | Opt2, MCS5 | — | -2.1 | — | dBm/ 3kHz |
| | | Opt2, MCS6 | — | -2.0 | — | dBm/ 3kHz |
| | | Opt3, MCS4 | — | 0.3 | — | dBm/ 3kHz |
| | | Opt3, MCS6 | — | 1.0 | — | dBm/ 3kHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Spectral Density (Average method per ANSI C63. 10-2020 11.10.3 AVGPSD-1) at frequency of highest level for a 3 kHz window with TX setting for $POUT_{12dBm}$ [1] [6] | $PSD_{3kHz\_12}$ | Opt1, MCS2 | — | -7.9 | — | dBm/ 3kHz |
| | | Opt1, MCS3 | — | -7.0 | — | dBm/ 3kHz |
| | | Opt1, MCS4 | — | -6.8 | — | dBm/ 3kHz |
| | | Opt1, MCS5 | — | -6.6 | — | dBm/ 3kHz |
| | | Opt1, MCS6 | — | -6.4 | — | dBm/ 3kHz |
| | | Opt2, MCS3 | — | -6.8 | — | dBm/ 3kHz |
| | | Opt2, MCS4 | — | -6.5 | — | dBm/ 3kHz |
| | | Opt2, MCS5 | — | -6.1 | — | dBm/ 3kHz |
| | | Opt2, MCS6 | — | -6.1 | — | dBm/ 3kHz |
| | | Opt3, MCS4 | — | -3.7 | — | dBm/ 3kHz |
| | | Opt3, MCS6 | — | -3.1 | — | dBm/ 3kHz |
| Adjacent Channel Power Ratio with TX setting for $POUT_{16dBm}$ per Wi-SUN Alliance [6] [7] | $ACPR_{WISUN}$ | Opt1, MCS2 | 20 | 22.3 | — | dBc |
| | | Opt1, MCS3 | 20 | 22.7 | — | dBc |
| | | Opt1, MCS4 | 20 | 22.8 | — | dBc |
| | | Opt1, MCS5 | 20 | 22.9 | — | dBc |
| | | Opt1, MCS6 | 20 | 23.0 | — | dBc |
| | | Opt2, MCS3 | 20 | 25.3 | — | dBc |
| | | Opt2, MCS4 | 20 | 25.6 | — | dBc |
| | | Opt2, MCS5 | 20 | 25.6 | — | dBc |
| | | Opt2, MCS6 | 20 | 25.8 | — | dBc |
| | | Opt3, MCS4 | 20 | 25.3 | — | dBc |
| | | Opt3, MCS6 | 20 | 25.4 | — | dBc |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Alternate Adjacent Channel Power Ratio with TX setting for $POUT_{16dBm}$ per Wi-SUN Alliance[6] [7] | $A2CPR_{WISUN}$ | Opt1, MCS2 | 40 | 49.6 | — | dBc |
| | | Opt1, MCS3 | 40 | 49.7 | — | dBc |
| | | Opt1, MCS4 | 40 | 49.7 | — | dBc |
| | | Opt1, MCS5 | 40 | 49.7 | — | dBc |
| | | Opt1, MCS6 | 40 | 49.6 | — | dBc |
| | | Opt2, MCS3 | 40 | 49.4 | — | dBc |
| | | Opt2, MCS4 | 40 | 49.5 | — | dBc |
| | | Opt2, MCS5 | 40 | 49.4 | — | dBc |
| | | Opt2, MCS6 | 40 | 48.4 | — | dBc |
| | | Opt3, MCS4 | 40 | 48.5 | — | dBc |
| | | Opt3, MCS6 | 40 | 48.5 | — | dBc |

**Note:**

1. With compliance to FCC Title 47 CFR Part 15.247, Wi-SUN Alliance PHY Working Group Technical Specification Revision 1VA9, and IEEE 802.15.4-2020 Section 20
2. Min/Max numbers are measured at typical voltage, at typical $F_{RANGE}$ frequency, and at $T_A$ = 25 °C.
3. Other operating conditions are kept at Typical values.
4. Measured at typical voltage and at typical $F_{RANGE}$ frequency
5. For 902 MHz ≤ $f_0$ ≤ 928 MHz the harmonics at 2*$f_0$, 7*$f_0$ and part of 6*$f_0$ will end up in the non-restricted bands. The other harmonics are in the restricted bands.
6. Emissions are measured at $T_A$ = 25 °C
7. All Operating Conditions are Typical / Nominal only in accordance to Wi-SUN Alliance PHY Working Group Technical Specification Revision 1VA9 section 8.2.7.

#### 4.9.2.3 866 MHz Band RF SUN OFDM Transmitter Characteristics

This table is for devices with an output power rating of +16 dBm using the 868 MHz Band matching network as shown in the typical connections section. $POUT_{14dBm}$[1] is marking the nominal TX setting which is targeting POUT = +14 dBm at typical conditions.

**Table 4.20. 866 MHz Band RF SUN OFDM Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 863.1 | 866.5 | 876 | MHz |
| Active TX Power for +14 dBm TX output power setting[1] | $POUT_{14dBm}$ | Opt4, MCS2 | — | 14.1 | — | dBm |
| | | Opt4, MCS4 | — | 14.1 | — | dBm |
| | | Opt4, MCS5 | — | 14.2 | — | dBm |
| | | Opt4, MCS6 | — | 14.1 | — | dBm |
| Error Vector Magnitude over process variation with TX setting for $POUT_{14dBm}$[1] | $EVM_{14dBm}$ | Opt4, MCS2 | — | -30.1 | — | dB |
| | | Opt4, MCS4 | — | -28.0 | — | dB |
| | | Opt4, MCS5 | — | -28.6 | — | dB |
| | | Opt4, MCS6 | — | -28.7 | — | dB |
| Error Vector Magnitude in to 2:1 VSWR Load over process variation, measured at worst case mis-match phase angle, with TX setting for $POUT_{14dBm}$[1] | $EVM_{VSWR2\_14}$ | Opt4, MCS2, 2:1 VSWR, $T_A$ = 25 °C | — | -26.3 | — | dB |
| | | Opt4, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -24.9 | — | dB |
| | | Opt4, MCS5, 2:1 VSWR, $T_A$ = 25 °C | — | -25.1 | — | dB |
| | | Opt4, MCS6, 2:1 VSWR, $T_A$ = 25 °C | — | -25.0 | — | dB |
| Minimum active TX Power[1] | $POUT_{MIN}$ | Opt4, MCS2 | — | -27.1 | — | dBm |
| | | Opt4, MCS4 | — | -27.1 | — | dBm |
| | | Opt4, MCS5 | — | -27.0 | — | dBm |
| | | Opt4, MCS6 | — | -27.0 | — | dBm |
| Max Step Size for TX Power setting for POUT between 0 dBm to +12 dBm | $POUT_{STEP}$ | VREGVDD = AVDD = PAVDD = 3.6 V, T = 25 °C | — | 0.1 | — | dB |
| Output power variation vs PAVDD supply voltage from 3.45 V to 3.8 V, with TX setting for $POUT_{14dBm}$ | $PVAR_{V\_14}$ | Opt4, MCS2 | — | 0.1 | — | dB |
| | | Opt4, MCS4 | — | 0.1 | — | dB |
| | | Opt4, MCS5 | — | 0.1 | — | dB |
| | | Opt4, MCS6 | — | 0.1 | — | dB |
| Peak to peak output power variation vs ambient Temperature -40 °C to +85 °C with TX setting for $POUT_{14dBm}$ | $PVAR_{T85\_14}$ | Opt4, MCS2 | — | 1.04 | — | dB |
| | | Opt4, MCS4 | — | 0.96 | — | dB |
| | | Opt4, MCS5 | — | 1.07 | — | dB |
| | | Opt4, MCS6 | — | 1.10 | — | dB |
| Peak to peak output power variation vs ambient Temperature +85 °C to +105 °C with TX setting for $POUT_{14dBm}$ | $PVAR_{T105\_14}$ | Opt4, MCS2 | — | 0.23 | — | dB |
| | | Opt4, MCS4 | — | 0.23 | — | dB |
| | | Opt4, MCS5 | — | 0.23 | — | dB |
| | | Opt4, MCS6 | — | 0.20 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output power variation vs frequency with TX setting for $POUT_{14dBm}$.Frequency test is at MIN, TYP, and MAX of $F_{RANGE}$ | $PVAR_{F\_14}$ | Opt4, MCS2 | — | 0.18 | — | dB |
| | | Opt4, MCS4 | — | 0.16 | — | dB |
| | | Opt4, MCS5 | — | 0.14 | — | dB |
| | | Opt4, MCS6 | — | 0.17 | — | dB |
| Spurious emissions at spur frequencies inside the bands in which the -54 dBm max limit applies, while the on channel desired signal is at POUT = +14 dBm tested at the highest and lowest operating channel frequency, conducted measurement with 100 kHz RBW[2] [3] [4] | $SPUR_{ETSI\_54}$ | Opt4, MCS2 | — | -59.9 | -54 | dBm |
| | | Opt4, MCS4 | — | -60.4 | -54 | dBm |
| | | Opt4, MCS5 | — | -60.9 | -54 | dBm |
| | | Opt4, MCS6 | — | -59.6 | -54 | dBm |
| Spurious emissions at spur frequencies below 1 GHz where the -36 dBm max limit applies, while on channel desired signal is at POUT = +14 dBm tested at the highest and lowest operating channel frequency, conducted measurement with 100 kHz RBW[2] [3] [5] | $SPUR_{ETSI\_36}$ | Opt4, MCS2 | — | -44.3 | -36 | dBm |
| | | Opt4, MCS4 | — | -44.2 | -36 | dBm |
| | | Opt4, MCS5 | — | -44.8 | -36 | dBm |
| | | Opt4, MCS6 | — | -45.6 | -36 | dBm |
| Spurious emissions at spur frequency above 1 GHz (including harmonics), and below 6 GHz, while on channel desired signal is at POUT = +14 dBm for highest and lowest operating channel frequency, conducted measurement with 1 MHz RBW[2] [3] | $SPUR_{ETSI\_1G6}$ | Opt4, MCS2 | — | -54.0 | -30 | dBm |
| | | Opt4, MCS4 | — | -55.4 | -30 | dBm |
| | | Opt4, MCS5 | — | -51.4 | -30 | dBm |
| | | Opt4, MCS6 | — | -54.0 | -30 | dBm |
| Adjacent Channel Power Ratio while on channel desired signal is at POUT = +14 dBm per Wi-SUN Alliance[3] [6] | $ACPR_{WISUN}$ | Opt4, MCS2 | 20 | 26.0 | — | dBc |
| | | Opt4, MCS4 | 20 | 26.2 | — | dBc |
| | | Opt4, MCS5 | 20 | 26.1 | — | dBc |
| | | Opt4, MCS6 | 20 | 26.5 | — | dBc |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Alternate Adjacent Channel Power Ratio while on channel desired signal is at POUT = +14 dBm per Wi-SUN Alliance[3] [6] | $A2CPR_{WISUN}$ | Opt4, MCS2 | 40 | 47.1 | — | dBc |
| | | Opt4, MCS4 | 40 | 47.0 | — | dBc |
| | | Opt4, MCS5 | 40 | 47.0 | — | dBc |
| | | Opt4, MCS6 | 40 | 47.0 | — | dBc |

**Note:**

1. With compliance to ETSI EN 300 220-1 v3.1.1, Wi-SUN Alliance PHY Working Group Technical Specification Revision 1VA9, and IEEE 802.15.4-2020 Section 20 except for max power limit
2. Per ETSI EN 300 220-1 v3.1.1 section 5.9.2 and 5.9.3, Table 19
3. Emissions are measured at $T_A$ = 25 °C
4. Spurious emissions inside any of the four frequency bands are limited to -54 dBm: 47 to 74 MHz; 87.5 to 118 MHz; 174 to 230 MHz; and 470 to 790 MHz
5. Spurious emissions which are below 1 GHz and outside of the four frequency bands (47 to 74 MHz; 87.5 to 118 MHz; 174 to 230 MHz; and 470 to 790 MHz) are limited to -36 dBm
6. All Operating Conditions are Typical / Nominal only in accordance to Wi-SUN Alliance PHY Working Group Technical Specification Revision 1VA9 section 8.2.7.

#### 4.9.2.4 490 MHz Band RF SUN OFDM Transmitter Characteristics

This table is for devices with an output power rating of +16 dBm using the 470 MHz Band matching network as shown in the typical connections section. $POUT_{16dBm}$ is marking the nominal TX setting which is targeting POUT = +16 dBm at typical conditions.

**Table 4.21. 490 MHz Band RF SUN OFDM Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 470 | 490 | 510 | MHz |
| Active TX Power for +16 dBm TX output power setting | $POUT_{16dBm}$ | Opt4, MCS2 | — | 16.0 | — | dBm |
| | | Opt4, MCS4 | — | 16.0 | — | dBm |
| | | Opt4, MCS5 | — | 16.1 | — | dBm |
| | | Opt4, MCS6 | — | 16.0 | — | dBm |
| Error Vector Magnitude over process variation with TX setting for $POUT_{16dBm}$ | $EVM_{16dBm}$ | Opt4, MCS2 | — | -30.2 | — | dB |
| | | Opt4, MCS4 | — | -27.4 | — | dB |
| | | Opt4, MCS5 | — | -27.7 | — | dB |
| | | Opt4, MCS6 | — | -27.8 | — | dB |
| Error Vector Magnitude in to 2:1 VSWR Load over process variation measured at worst case mis-match phase angle, with TX setting for $POUT_{16dBm}$ | $EVM_{VSWR2\_16}$ | Opt4, MCS2, 2:1 VSWR, $T_A$ = 25 °C | — | -24.5 | — | dB |
| | | Opt4, MCS4, 2:1 VSWR, $T_A$ = 25 °C | — | -23.3 | — | dB |
| | | Opt4, MCS5, 2:1 VSWR, $T_A$ = 25 °C | — | -23.4 | — | dB |
| | | Opt4, MCS6, 2:1 VSWR, $T_A$ = 25 °C | — | -23.1 | — | dB |
| Minimum active TX Power | $POUT_{MIN}$ | Opt4, MCS2 | — | -28.0 | — | dBm |
| | | Opt4, MCS4 | — | -27.9 | — | dBm |
| | | Opt4, MCS5 | — | -27.8 | — | dBm |
| | | Opt4, MCS6 | — | -27.7 | — | dBm |
| Output power variation vs PAVDD supply voltage from 3.45 V to 3.8 V, with TX setting for $POUT_{16dBm}$ | $PVAR_{V\_16}$ | Opt4, MCS2 | — | 0.1 | — | dB |
| | | Opt4, MCS4 | — | 0.1 | — | dB |
| | | Opt4, MCS5 | — | 0.1 | — | dB |
| | | Opt4, MCS6 | — | 0.1 | — | dB |
| Peak to peak output power variation vs ambient Temperature -40 °C to +85 °C, with TX setting for $POUT_{16dBm}$ | $PVAR_{T85\_16}$ | Opt4, MCS2 | — | 0.49 | — | dB |
| | | Opt4, MCS4 | — | 0.57 | — | dB |
| | | Opt4, MCS5 | — | 0.55 | — | dB |
| | | Opt4, MCS6 | — | 0.49 | — | dB |
| Peak to peak output power variation vs ambient Temperature +85 °C to +105 °C, with TX setting for $POUT_{16dBm}$ | $PVAR_{T105\_16}$ | Opt4, MCS2 | — | 0.1 | — | dB |
| | | Opt4, MCS4 | — | 0.1 | — | dB |
| | | Opt4, MCS5 | — | 0.1 | — | dB |
| | | Opt4, MCS6 | — | 0.1 | — | dB |
| Output power variation vs frequency with TX setting for $POUT_{16dBm}$. Frequency test is at MIN, TYP, and MAX of $F_{RANGE}$ | $PVAR_{F\_16}$ | Opt4, MCS2 | — | 1.2 | — | dB |
| | | Opt4, MCS4 | — | 1.2 | — | dB |
| | | Opt4, MCS5 | — | 1.2 | — | dB |
| | | Opt4, MCS6 | — | 1.2 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Harmonic emissions per China SRW Requirement, Section 2.1 (frequencies below 1GHz). $P_{OUT}$ = +16 dBm, 490 MHz[1] | $SPUR_{HARM1\_CN}$ | Opt4, MCS2 | — | -62.1 | — | dBm |
| | | Opt4, MCS4 | — | -62.8 | — | dBm |
| | | Opt4, MCS5 | — | -62.3 | — | dBm |
| | | Opt4, MCS6 | — | -62.9 | — | dBm |
| Harmonic emissions per China SRW Requirement, Section 2.1 (frequencies above 1GHz). $P_{OUT}$ = +16 dBm, 490 MHz[1] | $SPUR_{HARM2\_CN}$ | Opt4, MCS2 | — | -62.6 | — | dBm |
| | | Opt4, MCS4 | — | -62.6 | — | dBm |
| | | Opt4, MCS5 | — | -62.4 | — | dBm |
| | | Opt4, MCS6 | — | -62.5 | — | dBm |
| Spurious emissions per China SRW Requirement, Section 3 (48.5-72.5MHz, 76-108MHz, 167-223MHz, and 606-798MHz). $P_{OUT}$ = +16 dBm, 490 MHz[1] | $SPUR_{OOB1\_CN}$ | Opt4, MCS2 | — | -57.6 | — | dBm |
| | | Opt4, MCS4 | — | -57.7 | — | dBm |
| | | Opt4, MCS5 | — | -57.6 | — | dBm |
| | | Opt4, MCS6 | — | -57.9 | — | dBm |
| Spurious emissions per China SRW Requirement, Section 2.1 (other frequencies below 1GHz). $P_{OUT}$ = +16 dBm, 490 MHz[1] | $SPUR_{OOB2\_CN}$ | Opt4, MCS2 | — | -53.4 | — | dBm |
| | | Opt4, MCS4 | — | -52.5 | — | dBm |
| | | Opt4, MCS5 | — | -53.7 | — | dBm |
| | | Opt4, MCS6 | — | -53.1 | — | dBm |
| Spurious emissions per China SRW Requirement, Section 2.1 (frequencies above 1GHz). $P_{OUT}$ = +16 dBm, 490 MHz[1] | $SPUR_{OOB3\_CN}$ | Opt4, MCS2 | — | -63.0 | — | dBm |
| | | Opt4, MCS4 | — | -63.0 | — | dBm |
| | | Opt4, MCS5 | — | -62.8 | — | dBm |
| | | Opt4, MCS6 | — | -63.1 | — | dBm |
| Adjacent Channel Power Ratio while on channel desired signal is at POUT = +16 dBm per Wi-SUN Alliance[1] [2] | $ACPR_{WISUN}$ | Opt4, MCS2 | — | 24.2 | — | dBc |
| | | Opt4, MCS4 | — | 24.0 | — | dBc |
| | | Opt4, MCS5 | — | 24.2 | — | dBc |
| | | Opt4, MCS6 | — | 24.3 | — | dBc |
| Alternate Adjacent Channel Power Ratio while on channel desired signal is at POUT = +16 dBm per Wi-SUN Alliance[1] [2] | $A2CPR_{WISUN}$ | Opt4, MCS2 | — | 47.6 | — | dBc |
| | | Opt4, MCS4 | — | 47.7 | — | dBc |
| | | Opt4, MCS5 | — | 47.7 | — | dBc |
| | | Opt4, MCS6 | — | 47.8 | — | dBc |

**Note:**

1. Emissions are tested at $T_A$ = 25 °C.
2. All Operating Conditions are Typical / Nominal only in accordance to Wi-SUN Alliance PHY Working Group Technical Specification Revision 1VA9 section 8.2.7.

### 4.9.3 RF Proprietary Receiver Characteristics

#### 4.9.3.1 920 MHz Band RF Receiver Characteristics

Band is 922.3 to 928.1 MHz. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, external PA Supply, supply filtering as shown in the typical connections section, crystal frequency = 39.0 MHz ± 1 ppm, and RF center frequency 924.0 MHz.

**Table 4.22. 920 MHz Band RF Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 922.3 | 924 | 928.1 | MHz |
| Rx Max Strong Signal Input Level for PER 10% | $RX_{SAT}$ | Desired is reference 400 kbps 4FSK signal[1] | — | — | 10 | dBm |
| Sensitivity | SENS | Desired is reference 50 kbps 2FSK signal, Δf = ± 25 kHz, PER<10%[2] [3] | — | -109.9 | -108.6 | dBm |
| | | Desired is reference 50 kbps 2FSK signal, Δf = ± 25 kHz, PER<10%[2] | — | -109.9 | -106.4 | dBm |
| | | Desired is reference 100 kbps 2FSK signal, Δf = ± 50 kHz, PER<10%[4] [3] | — | -107.0 | -105.9 | dBm |
| | | Desired is reference 100 kbps 2FSK signal, Δf = ± 50 kHz, PER<10%[4] | — | -107.0 | -103.2 | dBm |
| | | Desired is reference 400 kbps 4FSK signal, $\Delta f_o$ = ± 100 kHz, $\Delta f_i$ = ± 33.3 kHz, PER<10%[1] | — | -99.1 | — | dBm |
| Adjacent channel rejection, Interferer is CW at ± 1 × channel spacing | ACR1 | Desired is reference 50 kbps 2FSK signal[2] at 3dB above sensitivity level | — | 45.4 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 46.9 | — | dB |
| | | Desired is reference 400 kbps 4FSK signal[1] at 3dB above sensitivity level | — | 42.1 | — | dB |
| Alternate channel rejection, Interferer is CW at ± 2 × channel spacing | ACR2 | Desired is reference 50 kbps 2FSK signal[2] at 3dB above sensitivity level | — | 50.8 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 55.4 | — | dB |
| | | Desired is reference 400 kbps 4FSK signal[1] at 3dB above sensitivity level | — | 47.1 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Image rejection, Interferer is CW at image frequency | IR | Desired is reference 50 kbps 2FSK signal[2] at 3dB above sensitivity level | — | 46.6 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 47.2 | — | dB |
| | | Desired is reference 400 kbps 4FSK signal[1] at 3dB above sensitivity level | — | 42.1 | — | |
| Blocking selectivity, 10% PER. Desired is 100 kbps 2FSK signal at 3dB above sensitivity level | BLOCK | Interferer CW at Desired ± 1 MHz | — | 55.2 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 62.9 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 78.6 | — | dB |
| Intermod selectivity,10% PER. CW interferers at 400 kHz and 800 kHz offsets | IM | Desired is reference 100 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 43.7 | — | dB |
| Upper limit of input power range over which $RSSI_{RES}$ and $RSSI_{ABSERR}$ are maintained | $RSSI_{MAX}$ | | — | — | -30 | dBm |
| Lower limit of input power range over which $RSSI_{RES}$ and $RSSI_{ABSERR}$ are maintained | $RSSI_{MIN}$ | | -100 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dB |
| RSSI maximum absolute error over typical conditions with offset correction | $RSSI_{ABSERR}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 1.6 | — | dB |
| Max spurious emissions during active receive mode, per ARIB STD-T108 Part 2, Section 3.3 | $SPUR_{RX\_ARIB}$ | Below 710 MHz, RBW = 100kHz | — | -84.5 | -54 | dBm |
| | | 710-900 MHz, RBW = 1MHz | — | -92.1 | -55 | dBm |
| | | 900-915 MHz, RBW = 100kHz | — | -102.6 | -55 | dBm |
| | | 915-930 MHz, RBW = 100kHz | — | -104.3 | -54 | dBm |
| | | 930-1000 MHz, RBW = 100kHz | — | -100.5 | -55 | dBm |
| | | Above 1000 MHz, RBW = 1MHz | — | -78.6 | -47 | dBm |

**Note:**

1. Definition of reference signal is 400 kbps 4FSK, BT = 2, mi = 0.33, PER<10%, Channel Spacing = 600 kHz, Data Whitening, no FEC, Per IEEE 802.15.4g 920 MHz band, mode 4.
2. Definition of reference signal is 50 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 200 kHz, Data Whitening, no FEC.
3. Min/Max numbers are measured at typical voltage, at typical $F_{RANGE}$ frequency, and at $T_A$ = 25 °C.
4. Definition of reference signal is 100 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 400 kHz, Data Whitening, no FEC.

#### 4.9.3.2 915 MHz Band RF Receiver Characteristics

Band is 902 to 928 MHz. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, crystal frequency = 39.0 MHz ± 1 ppm, supply filtering as shown in the typical connections section, and RF center frequency 915 MHz.

**Table 4.23. 915 MHz Band RF Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | — | 928 | MHz |
| Rx Max Strong Signal Input Level for 0.1% BER | $RX_{SAT}$ | Desired is reference 2 Mbps 2GFSK signal[1] | — | — | 10 | dBm |
| Sensitivity | SENS | Desired is reference 10 kbps 2GFSK signal, Δf = ± 5 kHz, PER<1%[2] | — | -117.0 | — | dBm |
| | | Desired is reference 50 kbps 2FSK signal, Δf = ± 25 kHz, PER<10%[3] | — | -109.9 | — | dBm |
| | | Desired is reference 50 kbps 2FSK signal, Δf = ± 25 kHz, PER<10% with FEC[4] | — | -114.6 | — | dBm |
| | | Desired is reference 150 kbps 2FSK signal, Δf = ± 37.5 kHz, PER<10%[5] | — | -106.8 | — | dBm |
| | | Desired is reference 2 Mbps 2GFSK signal, Δf = ± 500 kHz, BER<0.1%[1] | — | -96.9 | — | dBm |
| | | Desired is reference 4.8 kbps O-QPSK signal, spreading factor = 8, PER<1%[6] | — | -125.8 | — | dBm |
| | | Desired is reference 250 kbps O-QPSK DSSS signal, PER<1%[7] | — | -103.3 | — | dBm |
| Adjacent channel rejection, Interferer is CW at ± 1 × channel spacing | ACR1 | Desired is reference 50 kbps 2FSK signal[3] at 3dB above sensitivity level | — | 45.2 | — | dB |
| | | Desired is reference 150 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 45.5 | — | dB |
| | | Desired is reference 250 kbps O-QPSK DSSS signal[7] at 3dB above sensitivity level | — | 41.5 | — | dB |
| Alternate channel rejection, Interferer is CW at ± 2 × channel spacing | ACR2 | Desired is reference 50 kbps 2FSK signal[3] at 3dB above sensitivity level | — | 50.8 | — | dB |
| | | Desired is reference 150 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 56.1 | — | dB |
| | | Desired is reference 250 kbps O-QPSK DSSS signal[7] at 3dB above sensitivity level | — | 45.5 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Image rejection, Interferer is CW at image frequency | IR | Desired is reference 50 kbps 2FSK signal[3] at 3dB above sensitivity level | — | 45.2 | — | dB |
| | | Desired is reference 150 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 45.5 | — | dB |
| | | Desired is reference 250 kbps O-QPSK DSSS signal[7] at 3dB above sensitivity level | — | 43.3 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 1 MHz frequency offset. | $BLOCK_{1M}$ | 50 kbps 2FSK[3] | — | 63.5 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 2 MHz frequency offset. | $BLOCK_{2M}$ | 50 kbps 2FSK[3] | — | 71.4 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 10 MHz frequency offset. | $BLOCK_{10M}$ | 50 kbps 2FSK[3] | — | 82.0 | — | dB |
| Intermod selectivity, PER < 10%. CW interferers at 400 kHz and 800 kHz offsets | IM | Desired is reference 50 kbps 2GFSK signal[3] at 3dB above sensitivity level | — | 45.8 | — | dB |
| Upper limit of input power range over which $RSSI_{RES}$ and $RSSI_{ABSERR}$ are maintained | $RSSI_{MAX}$ | | — | — | -30 | dBm |
| Lower limit of input power range over which $RSSI_{RES}$ and $RSSI_{ABSERR}$ are maintained | $RSSI_{MIN}$ | | -100 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dB |
| RSSI maximum absolute error over typical conditions with offset correction | $RSSI_{ABSERR}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 1.2 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX\_FCC}$ | 216-960 MHz | — | -84.7 | -49.2 | dBm |
| | | Above 960 MHz | — | -76.5 | -41.2 | dBm |

**Note:**

1. Crystal tolerance = 0 ppm.
2. Definition of reference signal is 10 kbps 2GFSK, BT = 2, mi = 1.0, PER<1%, RX channel BW = 40 kHz, payload length = 20 octets.
3. Definition of reference signal is 50 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 200 kHz, Data Whitening, no FEC.
4. Definition of reference signal is 50 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 200 kHz, Data Whitening, with FEC.
5. Definition of reference signal is 150 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 400 kHz, Data Whitening, no FEC.
6. Definition of reference signal is 4.8 kbps O-QPSK DSSS long-range PHY, 38.4 kcps chip rate, chipping code length 32, PER<1%. Crystal tolerance = 0 ppm.
7. Definition of reference signal is O-QPSK DSSS, Data rate = 250 kbps, 32-chip PN sequence mapping, <1% PER, Channel Spacing = 2 MHz, payload length = 20 octets. Crystal tolerance = 0 ppm.

#### 4.9.3.3 868 MHz Band RF Receiver Characteristics

Band is 868 to 870 MHz. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, crystal frequency = 39.0 MHz ± 1 ppm, supply filtering as shown in the typical connections section, and RF center frequency 868.3 MHz.

**Table 4.24. 868 MHz Band RF Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 863 | — | 870 | MHz |
| Rx Max Strong Signal Input Level for 0.1% BER | $RX_{SAT}$ | Desired is reference 500 kbps 2GMSK signal[1] | — | — | 10 | dBm |
| Sensitivity | SENS | Desired is reference 10 kbps 2GFSK signal, Δf = ± 5 kHz, PER<10%[2] | — | -119.3 | — | dBm |
| | | Desired is reference 38.4 kbps 2GFSK signal, Δf = ± 20 kHz, BER<0.1%[3] | — | -113.2 | — | dBm |
| | | Desired is reference 50 kbps 2FSK signal, Δf = ± 12.5 kHz, PER<10%[4] | — | -110.8 | — | dBm |
| | | Desired is reference 100 kbps 2FSK signal, Δf = ± 25 kHz, PER<10%[5] | — | -108.0 | — | dBm |
| | | Desired is reference 500 kbps 2GMSK signal, Δf = ± 125 kHz[1], BER<0.1%[6] | — | -103.0 | — | dBm |
| | | Desired is reference 100 kbps O-QPSK DSSS signal, PER<1%[7] | — | -109.8 | — | dBm |
| Adjacent channel rejection, Interferer is CW at ± 1 × channel spacing | ACR1 | Desired is reference 10 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 53.3 | — | dB |
| | | Desired is reference 38.4 kbps 2GFSK signal[3] at 3dB above sensitivity level | — | 44.8 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 45.7 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 44.8 | — | dB |
| | | Desired is reference 100 kbps O-QPSK DSSS signal [7] at 3dB above sensitivity level | — | 56.3 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Alternate channel rejection, Interferer is CW at ± 2 × channel spacing | ACR2 | Desired is reference 10 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 53.7 | — | dB |
| | | Desired is reference 38.4 kbps 2GFSK signal[3] at 3dB above sensitivity level | — | 41.9 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 45.1 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 50.5 | — | dB |
| | | Desired is reference 100 kbps O-QPSK DSSS signal [7] at 3dB above sensitivity level | — | 67.1 | — | dB |
| Image rejection, Interferer is CW at image frequency | IR | Desired is reference 10 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 44.5 | — | dB |
| | | Desired is reference 38.4 kbps 2GFSK signal[3] at 3dB above sensitivity level | — | 42.0 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 46.8 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 46.2 | — | dB |
| | | Desired is reference 100 kbps O-QPSK DSSS signal [7] at 3dB above sensitivity level | — | 44.1 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 1 MHz frequency offset. | $BLOCK_{1M}$ | 50 kbps 2FSK signal[4] | — | 64.4 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 2 MHz frequency offset. | $BLOCK_{2M}$ | 50 kbps 2FSK signal[4] | — | 73.5 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 10 MHz frequency offset. | $BLOCK_{10M}$ | 50 kbps 2FSK signal[4] | — | 84.1 | — | dB |
| Upper limit of input power range over which $RSSI_{RES}$ and $RSSI_{ABSERR}$ are maintained | $RSSI_{MAX}$ | | — | — | -40 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Lower limit of input power range over which $RSSI_{RES}$ and $RSSI_{ABSERR}$ are maintained | $RSSI_{MIN}$ | | -100 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dB |
| RSSI maximum absolute error over typical conditions with offset correction | $RSSI_{ABSERR}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 1.8 | — | dB |
| Max spurious emissions during active receive mode | $SPUR_{RX}$ | 30 MHz to 1 GHz | — | -84.8 | -57 | dBm |
| | | 1 GHz to 6 GHz | — | -76.1 | -47 | dBm |

**Note:**

1. Definition of reference signal is 500 kbps 2GMSK, BT = 0.5, mi = 0.5, BER<0.1%, RX channel BW = 753.320 kHz. Crystal tolerance = 0 ppm.
2. Definition of reference signal is 10 kbps 2GFSK, BT = 0.5, mi = 1.0, PER<10%, Data Whitening, no FEC. Crystal tolerance = 0 ppm. Per IEEE 802.15.4x.
3. Definition of reference signal is 38.4 kbps 2GFSK, BT = 0.5, mi = 1.04, BER<0.1%, RX channel BW = 74.809 kHz, channel spacing = 100 kHz. Crystal tolerance = 0 ppm.
4. Definition of reference signal is 50 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 100 kHz, Data Whitening, no FEC.
5. Definition of reference signal is 100 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 200 kHz, Data Whitening, no FEC.
6. The modulation bandwidth may not be suitable for regional regulatory requirements in this band. Crystal tolerance = 0 ppm.
7. Definition of reference signal is O-QPSK DSSS per IEEE 802.15.4 section 12.2 and Table 12-2, Data rate = 100 kbps, 4 bit to 16 chip PN sequence mapping, <1% PER, Channel Spacing = 2 MHz, payload length = 20 octets.

#### 4.9.3.4 470 MHz Band RF Receiver Characteristics

Band is 470 to 510 MHz. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, supply filtering as shown in the typical connections section, crystal frequency = 39.0 MHz ± 1 ppm, and RF center frequency 490 MHz.

**Table 4.25. 470 MHz Band RF Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 470 | — | 510 | MHz |
| Rx Max Strong Signal Input Level for 10% PER | $RX_{SAT}$ | Desired is reference 100 kbps 2FSK signal[1] | — | — | 10 | dBm |
| Sensitivity | SENS | Desired is reference 10 kbps 2GFSK signal, Δf = ± 25 kHz, BER<0.1%[2] | — | -117.7 | — | dBm |
| | | Desired is reference 50 kbps 2FSK signal, Δf = ± 25 kHz, PER<10%[3] | — | -111.1 | — | dBm |
| | | Desired is reference 100 kbps 2FSK signal, Δf = ± 25 kHz, PER<10%[1] | — | -110.1 | — | dBm |
| Adjacent channel rejection, Interferer is CW at ± 1 × channel spacing | ACR1 | Desired is reference 10 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 52.2 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[3] at 3dB above sensitivity level | — | 48.7 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[1] at 3dB above sensitivity level | — | 46.4 | — | dB |
| Alternate channel rejection, Interferer is CW at ± 2 × channel spacing | ACR2 | Desired is reference 10 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 40.7 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[3] at 3dB above sensitivity level | — | 53.9 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[1] at 3dB above sensitivity level | — | 55.3 | — | dB |
| Image rejection, Interferer is CW at image frequency | IR | Desired is reference 10 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 40.5 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[3] at 3dB above sensitivity level | — | 49.1 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[1] at 3dB above sensitivity level | — | 48.0 | — | dB |
| Blocking selectivity, 0.1% BER. Desired is reference 10 kbps 2GFSK signal[2] at 3dB above sensitivity level | $BLOCK_{10}$ | Interferer CW at Desired ± 1 MHz | — | 72.4 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 80.1 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 86.0 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Upper limit of input power range over which $RSSI_{RES}$ and $RSSI_{ABSERR}$ are maintained | $RSSI_{MAX}$ | | — | — | -30 | dBm |
| Lower limit of input power range over which $RSSI_{RES}$ and $RSSI_{ABSERR}$ are maintained | $RSSI_{MIN}$ | | -100 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dB |
| RSSI maximum absolute error over typical conditions with offset correction | $RSSI_{ABSERR}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 2.3 | — | dB |
| Max spurious emissions during active receive mode | $SPUR_{RX}$ | 30 MHz to 1 GHz | — | -81.0 | -57 | dBm |
| | | 1 GHz to 10th Harmonic | — | -71.8 | -47 | dBm |

**Note:**

1. Definition of reference signal is 100 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 200 kHz.
2. Definition of reference signal is 10 kbps 2GFSK, BT = 0.5, mi = 5.0, BER<0.1%, RX channel BW = 99.2 kHz. Crystal tolerance = 0 ppm.
3. Definition of reference signal is 50 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 200 kHz.

#### 4.9.4 RF SUN O-QPSK Receiver Characteristics

SUN O-QPSK DSSS Modulations are defined by IEEE 802.15.4-2020 section 21, and Table 21-4 using the following abbreviations: Rc = baud or Chip rate (kchip/s), RM = Rate mode (index), Rd = bit data rate (kbps), and PL = PSDU Length (octets). Measurements use packet length of 250 octets when data rate is 50 kbps or higher, and 20 octets packet length when lower then 50 kbps.

#### 4.9.4.1 914 MHz Band RF SUN O-QPSK Receiver Characteristics

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, external PA Supply, supply filtering as shown in the typical connections section.

**Table 4.26. 914 MHz Band RF SUN O-QPSK Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | 914 | 928 | MHz |
| Rx Sensitivity for 10% Packet Error Rate (PER) with no interferer for SUN O-QPSK modulations | SENS | Rc = 100, RM = 0, Rd = 6.25 | — | -123.9 | — | dBm |
| | | Rc = 100, RM = 1, Rd = 12.5 | — | -121.1 | — | dBm |
| | | Rc = 100, RM = 2, Rd = 25 | — | -120.2 | — | dBm |
| | | Rc = 100, RM = 3, Rd = 50 | — | -118.8 | — | dBm |
| | | Rc = 1000, RM = 0, Rd = 31.25 | — | -116.0 | — | dBm |
| | | Rc = 1000, RM = 1, Rd = 125 | — | -113.1 | — | dBm |
| | | Rc = 1000, RM = 2, Rd = 250 | — | -110.6 | — | dBm |
| | | Rc = 1000, RM = 3, Rd = 500 | — | -109.0 | — | dBm |
| Rx Max Strong Signal Input Level for 10% PER | $RX_{SAT}$ | Rc = 100, RM = 0, Rd = 6.25 | — | 10 | — | dBm |
| | | Rc = 1000, RM = 3, Rd = 500 | — | 10 | — | dBm |
| Adjacent Channel Rejection is the U/D ratio in dB (a.k.a. ISR) for 10% PER according to IEEE 802.15.4-2020 section 21.5.4 for the lower \|Δf\| in table 21-23, with Desired signal at 3 dB above required sensitivity in Table 21-21.[1] | ACR1 | Rc = 100, RM = 0, Rd = 6.25 | — | 61.5 | — | dB |
| | | Rc = 100, RM = 1, Rd = 12.5 | — | 58.3 | — | dB |
| | | Rc = 100, RM = 2, Rd = 25 | — | 57.6 | — | dB |
| | | Rc = 100, RM = 3, Rd = 50 | — | 56.4 | — | dB |
| | | Rc = 1000, RM = 0, Rd = 31.25 | — | 55.3 | — | dB |
| | | Rc = 1000, RM = 1, Rd = 125 | — | 52.1 | — | dB |
| | | Rc = 1000, RM = 2, Rd = 250 | — | 49.7 | — | dB |
| | | Rc = 1000, RM = 3, Rd = 500 | — | 48.0 | — | dB |
| Alternate Adjacent Channel Rejection (ISR) is the U/D ratio in dB for 10% PER according to IEEE 802.15.4-2020 section 21.5.4 for the higher \|Δf\| in table 21-23, with Desired signal at 3 dB above required sensitivity in Table 21-21.[1] | ACR2 | Rc = 100, RM = 0, Rd = 6.25 | — | 71.1 | — | dB |
| | | Rc = 100, RM = 1, Rd = 12.5 | — | 68.0 | — | dB |
| | | Rc = 100, RM = 2, Rd = 25 | — | 67.3 | — | dB |
| | | Rc = 100, RM = 3, Rd = 50 | — | 65.5 | — | dB |
| | | Rc = 1000, RM = 0, Rd = 31.25 | — | 58.9 | — | dB |
| | | Rc = 1000, RM = 1, Rd = 125 | — | 55.8 | — | dB |
| | | Rc = 1000, RM = 2, Rd = 250 | — | 53.3 | — | dB |
| | | Rc = 1000, RM = 3, Rd = 500 | — | 51.6 | — | dB |
| Co-Channel Rejection U/D ratio. Set Desired signal to 3 dB above required sensitivity level according to IEEE 805.15.4-2020 section 21.5.3, Table 21-21. Undesired signal level shall be adjusted to make PER = 10%.[1] | CoChR | Rc = 100, RM = 0, Rd = 6.25 | — | 3.6 | — | dB |
| | | Rc = 100, RM = 1, Rd = 12.5 | — | 1.8 | — | dB |
| | | Rc = 100, RM = 2, Rd = 25 | — | 0.2 | — | dB |
| | | Rc = 100, RM = 3, Rd = 50 | — | -0.5 | — | dB |
| | | Rc = 1000, RM = 0, Rd = 31.25 | — | 5.7 | — | dB |
| | | Rc = 1000, RM = 1, Rd = 125 | — | 2.1 | — | dB |
| | | Rc = 1000, RM = 2, Rd = 250 | — | -0.6 | — | dB |
| | | Rc = 1000, RM = 3, Rd = 500 | — | -4.3 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Error for Rx Energy Detection, and AGC. Input signal comprising all zero bits according to IEEE 802.15.4-2020 section 21.2.2.2, as a continuous Preamble. Report the signal level delta: Rx measured signal level averaged over two Preambles of 56 bits minus the applied signal level.[2] | $AGC_{Pre}$ | Rc = 100, RM = 0, Rd = 6.25 | — | 0.7 | — | dB |
| | | Rc = 100, RM = 3, Rd = 50 | — | 0.6 | — | dB |
| | | Rc = 1000, RM = 0, Rd = 31.25 | — | 0.5 | — | dB |
| | | Rc = 1000, RM = 3, Rd = 500 | — | 0.5 | — | dB |
| Frequency Error Sensitivity. Receiver signal level for 10% PER with the desired signal's frequency offset by ± 50 ppm. | $SENS_{FE}$ | Rc = 100, RM = 0, Rd = 6.25 | — | -121.0 | — | dBm |
| | | Rc = 100, RM = 1, Rd = 12.5 | — | -117.1 | — | dBm |
| | | Rc = 100, RM = 2, Rd = 25 | — | -119.9 | — | dBm |
| | | Rc = 100, RM = 3, Rd = 50 | — | -118.3 | — | dBm |
| | | Rc = 1000, RM = 0, Rd = 31.25 | — | -116.1 | — | dBm |
| | | Rc = 1000, RM = 1, Rd = 125 | — | -113.1 | — | dBm |
| | | Rc = 1000, RM = 2, Rd = 250 | — | -110.6 | — | dBm |
| | | Rc = 1000, RM = 3, Rd = 500 | — | -108.8 | — | dBm |
| Signal Quality Estimate index [0-255] for SUN O-QPSK modulation with the given input signal condition as measured by the receiver with AGC active. | SQE | at SENS Rc = 100, RM = 2, Rd = 25 | — | 42 | — | index |
| | | 3 dB above SENS Rc = 100, RM = 2, Rd = 25 | — | 63 | — | index |
| | | 10 dB above SENS Rc = 100, RM = 2, Rd = 25 | — | 119 | — | index |
| | | at -97 dBm Rc = 100, RM = 2, Rd = 25 | — | 217 | — | index |
| | | at -97 dBm and ACR1 Rc = 100, RM = 2, Rd = 25 | — | 40 | — | index |
| | | at -40 dBm no interferer Rc = 100, RM = 2, Rd = 25 | — | 255 | — | index |
| | | at -40 dBm with a co-channel interferer level adjusted for 10% PER[1] Rc = 100, RM = 2, Rd = 25 | — | 163 | — | index |
| | | at $SENS_{FE}$ with 50 ppm Delta Rc = 100, RM = 2, Rd = 25 | — | 40 | — | index |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Receive Signal Strength Indicator in dB for SUN O-QPSK modulation with the given input signal condition as measured by the receiver with AGC active. | RSSI | at SENS Rc = 100, RM = 2, Rd = 25 | — | -117.4 | — | dBm |
| | | 3 dB above SENS Rc = 100, RM = 2, Rd = 25 | — | -115.6 | — | dBm |
| | | 10 dB above SENS Rc = 100, RM = 2, Rd = 25 | — | -109.4 | — | dBm |
| | | at -97 dBm Rc = 100, RM = 2, Rd = 25 | — | -96.7 | — | dBm |
| | | at -97 dBm and Undesired at ACR1 Rc = 100, RM = 2, Rd = 25 | — | -95.3 | — | dBm |
| | | at -40 dBm no interferer Rc = 100, RM = 2, Rd = 25 | — | -39.9 | — | dBm |
| | | at -40 dBm with a co-channel interferer level adjusted for 10% PER[1] Rc = 100, RM = 2, Rd = 25 | — | -40.2 | — | dBm |
| | | at $SENS_{FE}$ with 50 ppm Delta Rc = 100, RM = 2, Rd = 25 | — | -117.7 | — | dBm |

**Note:**

1. The undesired signal shall be a compliant SUN O-QPSK PHY PSDU according to IEEE 802.15.4-2020 section 21.5.4 containing a pseudo random bit sequence which is different from the desired signal. The undesired signal omits the SHR and PHR, uses chip-whitening, and the chip rate and spreading mode are the same as the desired signal.
2. The specification is less than ± 6 dB error at all power levels between 10 dB above required sensitivity to 50 dB above required sensitivity.

### 4.9.5 RF Wi-SUN FSK Receiver Characteristics

Wi-SUN FSK Modulations are defined in Wi-SUN Alliance PHY Working Group (PHYWG TPS) Wi-SUN PHY Technical Specification - Amendment 1VA9 November 2022. The PHY modulations in this table use BT = 2 and are indicated by (T, M, C) where T is the Phy Mode ID Type, and M is the Mode from PHY WG TPS Tables 2, 3, and 4. Also, C is the Channel Plan ID from PHY WG TPS Tables 6 and 7. The PHYWG TPS also references IEEE 802.15.4-2020 section 19 especially. Measurements use packet length of 250 octets when data rate is 50 kbps or higher, and 20 octets packet length when lower than 50 kbps.

The following table gives information about the different Wi-SUN FSK configurations that are supported by this device family. This section is meant to be informative, in case of any contradiction the Wi-SUN PHY TPS takes precedence.

**Table 4.27. FSK Modulation for Wi-SUN, BT = 2, 2 level FSK, with Data Whitening**

| Old FSK # 1V09 PHY Op Mode[1] | Wi-SUN PHY (Type[2], Mode[3], ChanPlanID[4]) | PhyModeID decimal[5] | Data Rate (kbps) | Operating Band (MHz) | Modulation Index[6] | Channel Bandwidth[7] (kHz) | Channel Spacing (kHz) | FEC Enabled[9] |
|---|---|---|---|---|---|---|---|---|
| #1a | (0, 1, 36) | 1 | 50 | 866 | 0.5 | 65 | 100 | No |
| #1b | (0, 2, 1) | 2 | 50 | 914 | 1 | 100 | 200 | No |
| #1b | (0, 2, 21) | 2 | 50 | 923 | 1 | 100 | 200 | No |
| #2a | (0, 3, 37) | 3 | 100 | 866 | 0.5 | 110 | 200 | No |
| #2a | (0, 3, 1) | 3 | 100 | 914 | 0.5 | 110 | 200 | No |
| #2b | (0, 4, 22) | 4 | 100 | 923 | 1 | 200 | 400 | No |
| #3 | (0, 5, 37) | 5 | 150 | 866 | 0.5 | 165 | 200[8] | No |
| #3 | (0, 5, 2) | 5 | 150 | 914 | 0.5 | 165 | 400 | No |
| #3 | (0, 5, 22) | 5 | 150 | 923 | 0.5 | 165 | 400 | No |
| #4a | (0, 6, 2) | 6 | 200 | 914 | 0.5 | 220 | 400 | No |
| #4b | (0, 7, 23) | 7 | 200 | 923 | 1 | 400 | 600 | No |
| #5 | (0, 8, 3) | 8 | 300 | 914 | 0.5 | 330 | 600 | No |
| #5 | (0, 8, 23) | 8 | 300 | 923 | 0.5 | 330 | 600 | No |
| #1a | (1, 1, 36) | 17 | 50 | 866 | 0.5 | 65 | 100 | NRNSC |
| #1b | (1, 2, 1) | 18 | 50 | 914 | 1 | 100 | 200 | NRNSC |
| #1b | (1, 2, 21) | 18 | 50 | 923 | 1 | 100 | 200 | NRNSC |
| #2a | (1, 3, 37) | 19 | 100 | 866 | 0.5 | 110 | 200 | NRNSC |
| #2a | (1, 3, 1) | 19 | 100 | 914 | 0.5 | 110 | 200 | NRNSC |
| #2b | (1, 4, 22) | 20 | 100 | 923 | 1 | 200 | 400 | NRNSC |
| #3 | (1, 5, 37) | 21 | 150 | 866 | 0.5 | 165 | 200[8] | NRNSC |
| #3 | (1, 5, 2) | 21 | 150 | 914 | 0.5 | 165 | 400 | NRNSC |
| #3 | (1, 5, 22) | 21 | 150 | 923 | 0.5 | 165 | 400 | NRNSC |
| #4a | (1, 6, 2) | 22 | 200 | 914 | 0.5 | 220 | 400 | NRNSC |
| #4b | (1, 7, 23) | 23 | 200 | 923 | 1 | 400 | 600 | NRNSC |
| #5 | (1, 8, 3) | 24 | 300 | 914 | 0.5 | 330 | 600 | NRNSC |

| Old FSK # 1V09 PHY Op Mode[1] | Wi-SUN PHY (Type[2], Mode[3], ChanPlanID[4]) | PhyModeID decimal[5] | Data Rate (kbps) | Operating Band (MHz) | Modulation Index[6] | Channel Bandwidth[7] (kHz) | Channel Spacing (kHz) | FEC Enabled[9] |
|---|---|---|---|---|---|---|---|---|
| #5 | (1, 8, 23) | 24 | 300 | 923 | 0.5 | 330 | 600 | NRNSC |

**Note:**

1. Wi-SUN FSK Phy Operating Mode # from PHYWG TPS 1V09 November 2022, Table 2.
2. Wi-SUN PHY Type follows PHYWG TPS 1VA9, Table 3.
3. Wi-SUN PHY Mode follows PHYWG TPS 1VA9, Table 4.
4. Wi-SUN FSK Operating Frequency channel plan follows PHYWG TPS 1VA9, Tables 6 and 7.
5. Wi-SUN FSK Phy Mode ID is from Wi-SUN Standard PHYWG TPS 1VA9, Tables 2, 3, and 4. See also Table 16 first and second column.
6. Viterbi DeMod is enabled when modulation index (mi) is less than 1.0, and disabled when mi is 1.0 or higher.
7. Approximation of the modulation signal occupied channel bandwidth for information purpose.
8. Europe Region uses smaller channel spacing
9. Modulations use interleaving only with FEC. Also, when FEC is used it must be NRNSC.

#### 4.9.5.1 923 MHz Band RF Wi-SUN FSK Receiver Characteristics

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, external PA Supply, supply filtering as shown in the typical connections section, crystal frequency = 39.0 MHz ± 1 ppm.

**Table 4.28. 923 MHz Band RF Wi-SUN FSK Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range[1] | $F_{RANGE}$ | | 922.3 | 923.x | 928.1 | MHz |
| Rx Max Strong Signal Input Level for 10% PER. | $RX_{SAT}$ | #5 = (1, 8, 23)[2], 300 kbps, mi = 0.5, with FEC[3] | — | 10 | — | dBm |
| Rx Sensitivity for 10% Packet Error Rate (PER) with no interferer | SENS | #2b = (0, 4, 22)[2], 100 kbps, mi = 1.0, no FEC[4] | — | -107.0 | -103.2 | dBm |
| | | #1b = (1, 2, 21)[2], 50 kbps, mi = 1.0, with FEC[5] | — | -114.5 | — | dBm |
| | | #2b = (1, 4, 22)[2], 100 kbps, mi = 1.0, with FEC[6] | — | -111.1 | -107.2 | dBm |
| | | #3 = (1, 5, 22)[2], 150 kbps, mi = 0.5, with FEC[7] | — | -109.4 | — | dBm |
| | | #4b = (1, 7, 23)[2], 200 kbps, mi = 1.0, with FEC[8] | — | -108.0 | — | dBm |
| | | #5 = (1, 8, 23)[2], 300 kbps, mi = 0.5, with FEC[3] | — | -106.4 | -101.2 | dBm |
| Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 19.6.8 with Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 1 × channel spacing. Requires IR Calibration. | ACR1 | #2b = (0, 4, 22)[2], 100 kbps, mi = 1.0, no FEC[4] | — | 46.9 | — | dB |
| | | #1b = (1, 2, 21)[2], 50 kbps, mi = 1.0, with FEC[5] | — | 49.9 | — | dB |
| | | #2b = (1, 4, 22)[2], 100 kbps, mi = 1.0, with FEC[6] | — | 49.9 | — | dB |
| | | #3 = (1, 5, 22)[2], 150 kbps, mi = 0.5, with FEC[7] | — | 48.6 | — | dB |
| | | #4b = (1, 7, 23)[2], 200 kbps, mi = 1.0, with FEC[8] | — | 50.9 | — | dB |
| | | #5 = (1, 8, 23)[2], 300 kbps, mi = 0.5, with FEC[3] | — | 50.0 | — | dB |
| Alternate Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 19.6.8 with Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 2 × channel spacing. Requires IR Calibration. | ACR2 | #2b = (0, 4, 22)[2], 100 kbps, mi = 1.0, no FEC[4] | — | 53.2 | — | dB |
| | | #1b = (1, 2, 21)[2], 50 kbps, mi = 1.0, with FEC[5] | — | 53.6 | — | dB |
| | | #2b = (1, 4, 22)[2], 100 kbps, mi = 1.0, with FEC[6] | — | 58.5 | — | dB |
| | | #3 = (1, 5, 22)[2], 150 kbps, mi = 0.5, with FEC[7] | — | 57.1 | — | dB |
| | | #4b = (1, 7, 23)[2], 200 kbps, mi = 1.0, with FEC[8] | — | 56.3 | — | dB |
| | | #5 = (1, 8, 23)[2], 300 kbps, mi = 0.5, with FEC[3] | — | 57.8 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Image Rejection U/D ratio for 10% PER. Undesired signal is CW at the RX image frequency. Desired signal is 3dB above required sensitivity level according to IEEE 802.15.4-2020 section 19.6.7. | IR | #2b = (0, 4, 22)[2], 100 kbps, mi = 1.0, no FEC[4] | — | 47.2 | — | dB |
| | | #1b = (1, 2, 21)[2], 50 kbps, mi = 1.0, with FEC[5] | — | 51.3 | — | dB |
| | | #2b = (1, 4, 22)[2], 100 kbps, mi = 1.0, with FEC[6] | — | 50.1 | — | dB |
| | | #3 = (1, 5, 22)[2], 150 kbps, mi = 0.5, with FEC[7] | — | 48.3 | — | dB |
| | | #4b = (1, 7, 23)[2], 200 kbps, mi = 1.0, with FEC[8] | — | 51.4 | — | dB |
| | | #5 = (1, 8, 23)[2], 300 kbps, mi = 0.5, with FEC[3] | — | 49.3 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity level according to IEEE 802.15.4-2020 section 19.6.7. Undesired signal is CW at ± 10 MHz frequency offset. | $BLOCK_{10M}$ | #2b = (0, 4, 22)[2], 100 kbps, mi = 1.0, no FEC[4] | — | 78.6 | — | dB |
| | | #2b = (1, 4, 22)[2], 100 kbps, mi = 1.0, with FEC[6] | — | 83.9 | — | dB |
| Co-Channel Rejection U/D ratio. Set Desired signal to 3 dB above required sensitivity level according to IEEE 805.15.4-2020 section 19.6.7. Undesired signal is CW with level adjusted to make PER = 10%. | CoChR | #2b = (0, 4, 22)[2], 100 kbps, mi = 1.0, no FEC[4] | — | -2.9 | — | dB |
| | | #1b = (1, 2, 21)[2], 50 kbps, mi = 1.0, with FEC[5] | — | -1.4 | — | dB |
| | | #2b = (1, 4, 22)[2], 100 kbps, mi = 1.0, with FEC[6] | — | -1.6 | — | dB |
| | | #3 = (1, 5, 22)[2], 150 kbps, mi = 0.5, with FEC[7] | — | -4.9 | — | dB |
| | | #4b = (1, 7, 23)[2], 200 kbps, mi = 1.0, with FEC[8] | — | -2.2 | — | dB |
| | | #5 = (1, 8, 23)[2], 300 kbps, mi = 0.5, with FEC[3] | — | -5.3 | — | dB |
| Rx Energy Detection Magnitude Error, and AGC, averaged over 8 repetitions of the Preamble Field.[9] | $AGC_{PreamME}$ | #1b, 50 kbps, mi = 1.0 | — | 1.0 | — | dB |
| | | #2b, 100 kbps, mi = 1.0 | — | 0.9 | — | dB |
| | | #3, 150 kbps, mi = 0.5 | — | 1.2 | — | dB |
| | | #4b, 200 kbps, mi = 1.0 | — | 1.1 | — | dB |
| | | #5, 300 kbps, mi = 0.5 | — | 1.2 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency Error Sensitivity. Receiver signal level for 10% PER with the desired signal's frequency offset by the given $F_{Err}$. | $SENS_{FE}$ | #2b = (0, 4, 22)[2], 100 kbps, mi = 1.0, no FEC[4]. $F_{Err}$ = ± 110 ppm | — | -106.5 | — | dBm |
| | | #1b = (1, 2, 21)[2], 50 kbps, mi = 1.0, with FEC[5]. $F_{Err}$ = ± 70 ppm | — | -109.7 | — | dBm |
| | | #2b = (1, 4, 22)[2], 100 kbps, mi = 1.0, with FEC[6]. $F_{Err}$ = ± 110 ppm | — | -107.4 | — | dBm |
| | | #3 = (1, 5, 22)[2], 150 kbps, mi = 0.5, with FEC[7]. $F_{Err}$ = ± 110 ppm | — | -109.3 | — | dBm |
| | | #4b = (1, 7, 23)[2], 200 kbps, mi = 1.0, with FEC[8]. $F_{Err}$ = ± 90 ppm | — | -108.0 | — | dBm |
| | | #5 = (1, 8, 23)[2], 300 kbps, mi = 0.5, with FEC[3]. $F_{Err}$ = ± 100 ppm | — | -106.1 | — | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Receive Signal Strength Indicator in dB for the given input signal condition as measured by the receiver with AGC active. | RSSI | at SENS #2b = (1, 4, 22)[2] | — | -111.1 | — | dBm |
| | | 3 dB above SENS #2b = (1, 4, 22)[2] | — | -108.3 | — | dBm |
| | | 10 dB above SENS #2b = (1, 4, 22)[2] | — | -101.4 | — | dBm |
| | | at -91 dBm, #2b = (1, 4, 22)[2] | — | -91.8 | — | dBm |
| | | at -91 dBm and ACR1 #2b = (1, 4, 22)[2] | — | -90.4 | — | dBm |
| | | at -40 dBm no interferer #2b = (1, 4, 22)[2] | — | -40.7 | — | dBm |
| | | at -40 dBm with a co-channel CW interferer level adjusted for 10% PER #2b = (1, 4, 22)[2] | — | -39.5 | — | dBm |
| | | at $SENS_{FE}$ #2b = (1, 4, 22)[2]; $F_{Err}$ = ± 110 ppm | — | -107.7 | — | dBm |

**Note:**

1. Test Frequency F for Typ conditions varies slightly according to the PHY Channel Plan ID: F = 923.6 MHz for 21, F = 923.7 MHz for 22, and F = 923.8 MHz for 23.
2. The indexes provided inside the parenthesis for each Test Conditions description are (T, M, C) and these define the PHY being tested according to Wi-SUN PHYWG TPS amendment 1VA9 with T = Type ID in Table 3, M = Mode ID in Table 4, and C = Channel Plan ID in Tables 6 and 7. 4.9.5 RF Wi-SUN FSK Receiver Characteristics summarizes the options listed in this document.
3. Reference signal is 300 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 600 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #5
4. Reference signal is 100 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 400 kHz, Data Whitening, without FEC. Per Wi-SUN FAN PHY 1.0 standard mode #2b
5. Reference signal is 50 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 200 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #1b
6. Reference signal is 100 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 400 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #2b
7. Reference signal is 150 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 400 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #3
8. Reference signal is 100 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 600 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #4b
9. Using Preamble Field signal (section 19.2.3.1 of IEEE 802.15.4-2020), sweep Antenna input level in 2 dB steps starting from 10 dB above required sensitivity to 50 dB above required sensitivity of 802.15.4-2020 section 19.6.7 . At each 2 dB step, record the input signal level at the 50 Ω Antenna port along with the signal level measured by the receiver averaged over 8 Preamble Fields. The Magnitude Error is the absolute value of the difference between these two at the 2 dB step with the worst Error. AGC_PreamME = Max( |Avg(Rx_meas) - Rx_applied| ).

#### 4.9.5.2 914 MHz Band RF Wi-SUN FSK Receiver Characteristics

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, external PA Supply, supply filtering as shown in the typical connections section, crystal frequency = 39.0 MHz ± 1 ppm.

**Table 4.29. 914 MHz Band RF Wi-SUN FSK Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | 914 | 928 | MHz |
| Rx Max Strong Signal Input Level for 10% PER. | $RX_{SAT}$ | #5 = (1, 8, 3)[1], 300 kbps, mi = 0.5, with FEC[2] | — | 10 | — | dBm |
| Rx Sensitivity for 10% Packet Error Rate (PER) with no interferer | SENS | #1b = (0, 2, 1)[1], 50 kbps, mi = 1.0, no FEC[3] | — | -109.9 | — | dBm |
| | | #1b = (1, 2, 1)[1], 50 kbps, mi = 1.0, with FEC[4] | — | -114.6 | -110.5 | dBm |
| | | #2a = (1, 3, 1)[1], 100 kbps, mi = 0.5, with FEC[5] | — | -110.9 | — | dBm |
| | | #3 = (1, 5, 2)[1], 150 kbps, mi = 0.5, with FEC[6] | — | -109.4 | -104.1 | dBm |
| | | #4a = (1, 6, 2)[1], 200 kbps, mi = 0.5, with FEC[7] | — | -108.1 | -104.5 | dBm |
| | | #5 = (1, 8, 3)[1], 300 kbps, mi = 0.5, with FEC[2] | — | -106.4 | — | dBm |
| Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 19.6.8 with Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 1 × channel spacing. Requires IR Calibration. | ACR1 | #1b = (0, 2, 1)[1], 50 kbps, mi = 1.0, no FEC[3] | — | 45.2 | — | dB |
| | | #1b = (1, 2, 1)[1], 50 kbps, mi = 1.0, with FEC[4] | — | 49.5 | — | dB |
| | | #2a = (1, 3, 1)[1], 100 kbps, mi = 0.5, with FEC[5] | — | 46.3 | — | dB |
| | | #3 = (1, 5, 2)[1], 150 kbps, mi = 0.5, with FEC[6] | — | 48.2 | — | dB |
| | | #4a = (1, 6, 2)[1], 200 kbps, mi = 0.5, with FEC[7] | — | 48.1 | — | dB |
| | | #5 = (1, 8, 3)[1], 300 kbps, mi = 0.5, with FEC[2] | — | 49.3 | — | dB |
| Alternate Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 19.6.8 with Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 2 × channel spacing. Requires IR Calibration. | ACR2 | #1b = (0, 2, 1)[1], 50 kbps, mi = 1.0, no FEC[3] | — | 51.0 | — | dB |
| | | #1b = (1, 2, 1)[1], 50 kbps, mi = 1.0, with FEC[4] | — | 53.4 | — | dB |
| | | #2a = (1, 3, 1)[1], 100 kbps, mi = 0.5, with FEC[5] | — | 50.6 | — | dB |
| | | #3 = (1, 5, 2)[1], 150 kbps, mi = 0.5, with FEC[6] | — | 57.3 | — | dB |
| | | #4a = (1, 6, 2)[1], 200 kbps, mi = 0.5, with FEC[7] | — | 55.9 | — | dB |
| | | #5 = (1, 8, 3)[1], 300 kbps, mi = 0.5, with FEC[2] | — | 57.2 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Image Rejection U/D ratio for 10% PER. Undesired signal is CW at the RX image frequency. Desired signal is 3dB above required sensitivity level according to IEEE 802.15.4-2020 section 19.6.7. | IR | #1b = (0, 2, 1)[1], 50 kbps, mi = 1.0, no FEC[3] | — | 46.8 | — | dB |
| | | #1b = (1, 2, 1)[1], 50 kbps, mi = 1.0, with FEC[4] | — | 51.4 | — | dB |
| | | #2a = (1, 3, 1)[1], 100 kbps, mi = 0.5, with FEC[5] | — | 48.7 | — | dB |
| | | #3 = (1, 5, 2)[1], 150 kbps, mi = 0.5, with FEC[6] | — | 48.1 | — | dB |
| | | #4a = (1, 6, 2)[1], 200 kbps, mi = 0.5, with FEC[7] | — | 48.3 | — | dB |
| | | #5 = (1, 8, 3)[1], 300 kbps, mi = 0.5, with FEC[2] | — | 48.5 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity level according to IEEE 802.15.4-2020 section 19.6.7. Undesired signal is CW at ± 10 MHz frequency offset. | $BLOCK_{10M}$ | #1b = (0, 2, 1)[1], 50 kbps, mi = 1.0, no FEC[3] | — | 82.0 | — | dB |
| | | #1b = (1, 2, 1)[1], 50 kbps, mi = 1.0, with FEC[4] | — | 87.1 | — | dB |
| Co-Channel Rejection U/D ratio. Set Desired signal to 3 dB above required sensitivity level according to IEEE 805.15.4-2020 section 19.6.7. Undesired signal is CW with level adjusted to make PER = 10%. | CoChR | #1b = (0, 2, 1)[1], 50 kbps, mi = 1.0, no FEC[3] | — | -2.6 | — | dB |
| | | #1b = (1, 2, 1)[1], 50 kbps, mi = 1.0, with FEC[4] | — | -1.3 | — | dB |
| | | #2a = (1, 3, 1)[1], 100 kbps, mi = 0.5, with FEC[5] | — | -5.6 | — | dB |
| | | #3 = (1, 5, 2)[1], 150 kbps, mi = 0.5, with FEC[6] | — | -4.7 | — | dB |
| | | #4a = (1, 6, 2)[1], 200 kbps, mi = 0.5, with FEC[7] | — | -5.1 | — | dB |
| | | #5 = (1, 8, 3)[1], 300 kbps, mi = 0.5, with FEC[2] | — | -5.4 | — | dB |
| Rx Energy Detection Magnitude Error, and AGC, averaged over 8 repetitions of the Preamble Field.[8] | $AGC_{PreamME}$ | #1b, 50 kbps, mi = 1.0 | — | 1.4 | — | dB |
| | | #2a, 100 kbps, mi = 0.5 | — | 2.3 | — | dB |
| | | #3, 150 kbps, mi = 0.5 | — | 1.8 | — | dB |
| | | #4a, 200 kbps, mi = 0.5 | — | 1.9 | — | dB |
| | | #5, 300 kbps, mi = 0.5 | — | 1.4 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency Error Sensitivity. Receiver signal level for 10% PER with the desired signal's frequency offset by the given $F_{Err}$. | $SENS_{FE}$ | #1b = (0, 2, 1)[1], 50 kbps, mi = 1.0, no FEC[3]. $F_{Err}$ = ± 60 ppm | — | -109.0 | — | dBm |
| | | #1b = (1, 2, 1)[1], 50 kbps, mi = 1.0, with FEC[4]. $F_{Err}$ = ± 60 ppm | — | -109.7 | — | dBm |
| | | #2a = (1, 3, 1)[1], 100 kbps, mi = 0.5, with FEC[5]. $F_{Err}$ = ± 60 ppm | — | -108.6 | — | dBm |
| | | #3 = (1, 5, 2)[1], 150 kbps, mi = 0.5, with FEC[6]. $F_{Err}$ = ± 90 ppm | — | -106.8 | — | dBm |
| | | #4a = (1, 6, 2)[1], 200 kbps, mi = 0.5, with FEC[7]. $F_{Err}$ = ± 110 ppm | — | -106.2 | — | dBm |
| | | #5 = (1, 8, 3)[1], 300 kbps, mi = 0.5, with FEC[2]. $F_{Err}$ = ± 110 ppm | — | -106.0 | — | dBm |
| Receive Signal Strength Indicator in dB for the given input signal condition as measured by the receiver with AGC active. | RSSI | at SENS #3 = (1, 5, 2)[1] | — | -109.6 | — | dBm |
| | | 3 dB above SENS #3 = (1, 5, 2)[1] | — | -106.2 | — | dBm |
| | | 10 dB above SENS #3 = (1, 5, 2)[1] | — | -99.2 | — | dBm |
| | | at -89 dBm, #3 = (1, 5, 2)[1] | — | -89.6 | — | dBm |
| | | at -89 dBm and ACR1 #3 = (1, 5, 2)[1] | — | -89.4 | — | dBm |
| | | at -40 dBm no interferer, #3 = (1, 5, 2)[1] | — | -40.4 | — | dBm |
| | | at -40 dBm with a co-channel CW interferer level adjusted for 10% PER #3 = (1, 5, 2)[1] | — | -40.4 | — | dBm |
| | | at $SENS_{FE}$ #3 = (1, 5, 2)[1]; $F_{Err}$ = ± 90 ppm | — | -107.0 | — | dBm |

**Note:**

1. The indexes provided inside the parenthesis for each Test Conditions description are (T, M, C) and these define the PHY being tested according to Wi-SUN PHYWG TPS amendment 1VA9 with T = Type ID in Table 3, M = Mode ID in Table 4, and C = Channel Plan ID in Tables 6 and 7. 4.9.5 RF Wi-SUN FSK Receiver Characteristics summarizes the options listed in this document.
2. Reference signal is 300 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 600 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #5
3. Reference signal is 50 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 200 kHz, Data Whitening, without FEC. Per Wi-SUN FAN PHY 1.0 standard mode #1b
4. Reference signal is 50 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 200 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #1b
5. Reference signal is 100 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 200 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #2a
6. Reference signal is 150 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 400 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #3
7. Reference signal is 200 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 400 kHz, Data Whitening, without FEC. Per Wi-SUN FAN PHY 1.0 standard mode #4a
8. Using Preamble Field signal (section 19.2.3.1 of IEEE 802.15.4-2020), sweep Antenna input level in 2 dB steps starting from 10 dB above required sensitivity to 50 dB above required sensitivity of 802.15.4-2020 section 19.6.7 . At each 2 dB step, record the input signal level at the 50 Ω Antenna port along with the signal level measured by the receiver averaged over 8 Preamble Fields. The Magnitude Error is the absolute value of the difference between these two at the 2 dB step with the worst Error. AGC_PreamME = Max( |Avg(Rx_meas) - Rx_applied| ).

#### 4.9.5.3 866 MHz Band RF Wi-SUN FSK Receiver Characteristics

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = PAVDD = AVDD = 3.3 V, DVDD = IOVDD0-2 = RFVDD = 1.8 V from DC-DC regulator output, external PA Supply, supply filtering as shown in the typical connections section, crystal frequency = 39.0 MHz ± 1 ppm.

**Table 4.30. 866 MHz Band RF Wi-SUN FSK Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 863 | 866.5 | 876 | MHz |
| Rx Max Strong Signal Input Level for 10% PER. | $RX_{SAT}$ | #3 = (1, 5, 37)[1], 150 kbps, mi = 0.5, with FEC[2] | — | 10 | — | dBm |
| Rx Sensitivity for 10% Packet Error Rate (PER) with no interferer | SENS | #1a = (0, 1, 36)[1], 50 kbps, mi = 0.5, no FEC[3] | — | -110.8 | — | dBm |
| | | #2a = (0, 3, 37)[1], 100 kbps, mi = 0.5, no FEC[4] | — | -108.0 | — | dBm |
| | | #1a = (1, 1, 36)[1], 50 kbps, mi = 0.5, with FEC[5] | — | -114.1 | — | dBm |
| | | #2a = (1, 3, 37)[1], 100 kbps, mi = 0.5, with FEC[6] | — | -110.2 | — | dBm |
| | | #3 = (1, 5, 37)[1], 150 kbps, mi = 0.5, with FEC[2] | — | -108.8 | — | dBm |
| Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 19.6.8 with Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 1 × channel spacing. Requires IR Calibration. | ACR1 | #1a = (0, 1, 36)[1], 50 kbps, mi = 0.5, no FEC[3] | — | 45.7 | — | dB |
| | | #2a = (0, 3, 37)[1], 100 kbps, mi = 0.5, no FEC[4] | — | 44.8 | — | dB |
| | | #1a = (1, 1, 36)[1], 50 kbps, mi = 0.5, with FEC[5] | — | 49.3 | — | dB |
| | | #2a = (1, 3, 37)[1], 100 kbps, mi = 0.5, with FEC[6] | — | 46.9 | — | dB |
| | | #3 = (1, 5, 37)[1], 150 kbps, mi = 0.5, with FEC[2] | — | 45.5 | — | dB |
| Alternate Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 19.6.8 with Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 2 × channel spacing. Requires IR Calibration. | ACR2 | #1a = (0, 1, 36)[1], 50 kbps, mi = 0.5, no FEC[3] | — | 45.1 | — | dB |
| | | #2a = (0, 3, 37)[1], 100 kbps, mi = 0.5, no FEC[4] | — | 50.5 | — | dB |
| | | #1a = (1, 1, 36)[1], 50 kbps, mi = 0.5, with FEC[5] | — | 48.1 | — | dB |
| | | #2a = (1, 3, 37)[1], 100 kbps, mi = 0.5, with FEC[6] | — | 51.5 | — | dB |
| | | #3 = (1, 5, 37)[1], 150 kbps, mi = 0.5, with FEC[2] | — | 47.2 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Image Rejection U/D ratio for 10% PER. Undesired signal is CW at the RX image frequency. Desired signal is 3dB above required sensitivity level according to IEEE 802.15.4-2020 section 19.6.7. | IR | #1a = (0, 1, 36)[1], 50 kbps, mi = 0.5, no FEC[3] | — | 46.8 | — | dB |
| | | #2a = (0, 3, 37)[1], 100 kbps, mi = 0.5, no FEC[4] | — | 46.2 | — | dB |
| | | #1a = (1, 1, 36)[1], 50 kbps, mi = 0.5, with FEC[5] | — | 49.8 | — | dB |
| | | #2a = (1, 3, 37)[1], 100 kbps, mi = 0.5, with FEC[6] | — | 48.6 | — | dB |
| | | #3 = (1, 5, 37)[1], 150 kbps, mi = 0.5, with FEC[2] | — | 47.8 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity level according to IEEE 802.15.4-2020 section 19.6.7. Undesired signal is CW at ± 10 MHz frequency offset. | $BLOCK_{10M}$ | #1a = (0, 1, 36)[1], 50 kbps, mi = 0.5, no FEC[3] | — | 84.1 | — | dB |
| | | #1a = (1, 1, 36)[1], 50 kbps, mi = 0.5, with FEC[5] | — | 87.0 | — | dB |
| Co-Channel Rejection U/D ratio. Set Desired signal to 3 dB above required sensitivity level according to IEEE 805.15.4-2020 section 19.6.7. Undesired signal is CW with level adjusted to make PER = 10%. | CoChR | #1a = (0, 1, 36)[1], 50 kbps, mi = 0.5, no FEC[3] | — | -7.1 | — | dB |
| | | #2a = (0, 3, 37)[1], 100 kbps, mi = 0.5, no FEC[4] | — | -7.2 | — | dB |
| | | #1a = (1, 1, 36)[1], 50 kbps, mi = 0.5, with FEC[5] | — | -4.4 | — | dB |
| | | #2a = (1, 3, 37)[1], 100 kbps, mi = 0.5, with FEC[6] | — | -5.2 | — | dB |
| | | #3 = (1, 5, 37)[1], 150 kbps, mi = 0.5, with FEC[2] | — | -4.4 | — | dB |
| Rx Energy Detection Magnitude Error, and AGC, averaged over 8 repetitions of the Preamble Field.[7] | $AGC_{PreamME}$ | #1a, 50 kbps, mi = 0.5 | — | 1.1 | — | dB |
| | | #2a, 100 kbps, mi = 0.5 | — | 1.8 | — | dB |
| | | #3, 150 kbps, mi = 0.5 | — | 1.4 | — | dB |
| Frequency Error Sensitivity. Receiver signal level for 10% PER with the desired signal's frequency offset by the given $F_{Err}$. | $SENS_{FE}$ | #1a = (0, 1, 36)[1], 50 kbps, mi = 0.5, no FEC[3]. $F_{Err}$ = ± 60 ppm | — | -107.1 | — | dBm |
| | | #2a = (0, 3, 37)[1], 100 kbps, mi = 0.5, no FEC[4]. $F_{Err}$ = ± 60 ppm | — | -105.9 | — | dBm |
| | | #1a = (1, 1, 36)[1], 50 kbps, mi = 0.5, with FEC[5]. $F_{Err}$ = ± 60 ppm | — | -107.3 | — | dBm |
| | | #2a = (1, 3, 37)[1], 100 kbps, mi = 0.5, with FEC[6]. $F_{Err}$ = ± 60 ppm | — | -108.3 | — | dBm |
| | | #3 = (1, 5, 37)[1], 150 kbps, mi = 0.5, with FEC[2]. $F_{Err}$ = ± 90 ppm | — | -106.6 | — | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Receive Signal Strength Indicator in dB for the given input signal condition as measured by the receiver with AGC active. | RSSI | at SENS #2a = (1, 3, 37)[1] | — | -110.7 | — | dBm |
| | | 3 dB above SENS #2a = (1, 3, 37)[1] | — | -107.9 | — | dBm |
| | | 10 dB above SENS #2a = (1, 3, 37)[1] | — | -100.8 | — | dBm |
| | | at -91 dBm, #2a = (1, 3, 37)[1] | — | -92.2 | — | dBm |
| | | at -91 dBm and ACR1 #2a = (1, 3, 37)[1] | — | -91.7 | — | dBm |
| | | at -40 dBm no interferer #2a = (1, 3, 37)[1] | — | -41.1 | — | dBm |
| | | at -40 dBm with a co-channel CW interferer level adjusted for 10% PER #2a = (1, 3, 37)[1] | — | -41.0 | — | dBm |
| | | at $SENS_{FE}$ #2a = (1, 3, 37)[1]; $F_{Err}$ = ± 60 ppm | — | -109.2 | — | dBm |

**Note:**

1. The indexes provided inside the parenthesis for each Test Conditions description are (T, M, C) and these define the PHY being tested according to Wi-SUN PHYWG TPS amendment 1VA9 with T = Type ID in Table 3, M = Mode ID in Table 4, and C = Channel Plan ID in Tables 6 and 7. 4.9.5 RF Wi-SUN FSK Receiver Characteristics summarizes the options listed in this document.
2. Reference signal is 150 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 200 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #3
3. Reference signal is 50 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 100 kHz, Data Whitening, without FEC. Per Wi-SUN FAN PHY 1.0 standard mode #1a
4. Reference signal is 100 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 200 kHz, Data Whitening, without FEC. Per Wi-SUN FAN PHY 1.0 standard mode #2a
5. Reference signal is 50 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 100 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #1a
6. Reference signal is 100 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 200 kHz, Data Whitening, with FEC. Per Wi-SUN FAN PHY 1.0 standard mode #2a
7. Using Preamble Field signal (section 19.2.3.1 of IEEE 802.15.4-2020), sweep Antenna input level in 2 dB steps starting from 10 dB above required sensitivity to 50 dB above required sensitivity of 802.15.4-2020 section 19.6.7 . At each 2 dB step, record the input signal level at the 50 Ω Antenna port along with the signal level measured by the receiver averaged over 8 Preamble Fields. The Magnitude Error is the absolute value of the difference between these two at the 2 dB step with the worst Error. AGC_PreamME = Max( |Avg(Rx_meas) - Rx_applied| ).

### 4.9.6 RF SUN OFDM Receiver Characteristics

OFDM Modulation is defined in Wi-SUN Alliance PHY Working Group (PHYWG TPS) Wi-SUN PHY Technical Specification - Amendment 1VA9 November 2022 which refers to IEEE 802.15.4-2020 especially section 20.3 . In this table the indication "OptX, MCSy" means X as the Option number 1 through 4, and y is the MCS index 0 through 6, and PL is the Packet PPDU Length in octets. Unless otherwise specified, for OFDM Options 1 and 2 header is normally MCS0, for Option 3 header is normally MCS1, and for Option 4 header is normally MCS2. Measurements use packet length of 250 octets when data rate is 50 kbps or higher, and 20 octets packet length when lower than 50 kbps.

#### 4.9.6.1 923 MHz Band RF SUN OFDM Receiver Characteristics

**Table 4.31. 923 MHz Band RF SUN OFDM Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range[1] | $F_{RANGE}$ | | 922.3 | 923.x | 928.1 | MHz |
| Rx Sensitivity for 10% Packet Error Rate (PER) with no interferer | SENS | 923.5 MHz, Opt2, MCS0[2] | — | -113.0 | -111.3 | dBm |
| | | 923.5 MHz, Opt2, MCS0 | — | -113.0 | -108.3 | dBm |
| | | 923.5 MHz, Opt2, MCS1 | — | -112.1 | — | dBm |
| | | 923.5 MHz, Opt2, MCS2 | — | -109.9 | — | dBm |
| | | 923.5 MHz, Opt2, MCS3[2] | — | -107.3 | -106.0 | dBm |
| | | 923.5 MHz, Opt2, MCS3 | — | -107.3 | -103.1 | dBm |
| | | 923.5 MHz, Opt2, MCS4 | — | -104.8 | — | dBm |
| | | 923.5 MHz, Opt2, MCS5 | — | -102.0 | — | dBm |
| | | 923.5 MHz, Opt2, MCS6[2] | — | -98.4 | -97.3 | dBm |
| | | 923.5 MHz, Opt2, MCS6 | — | -98.4 | -94.3 | dBm |
| | | 923.7 MHz, Opt3, MCS0, header MCS0, with PL = 20 octets[2] | — | -115.0 | -113.1 | dBm |
| | | 923.7 MHz, Opt3, MCS0, header MCS0, with PL = 20 octets | — | -115.0 | -110.2 | dBm |
| | | 923.7 MHz, Opt3, MCS1, header MCS1[2] | — | -114.3 | -112.7 | dBm |
| | | 923.7 MHz, Opt3, MCS1, header MCS1 | — | -114.3 | -109.3 | dBm |
| | | 923.7 MHz, Opt3, MCS2[2] | — | -112.1 | -110.6 | dBm |
| | | 923.7 MHz, Opt3, MCS2 | — | -112.1 | -107.4 | dBm |
| | | 923.7 MHz, Opt3, MCS3[2] | — | -109.9 | -108.1 | dBm |
| | | 923.7 MHz, Opt3, MCS3 | — | -109.9 | -105.4 | dBm |
| | | 923.7 MHz, Opt3, MCS4[2] | — | -107.5 | -106.2 | dBm |
| | | 923.7 MHz, Opt3, MCS4 | — | -107.5 | -103.2 | dBm |
| | | 923.7 MHz, Opt3, MCS5[2] | — | -104.9 | -103.2 | dBm |
| | | 923.7 MHz, Opt3, MCS5 | — | -104.9 | -100.1 | dBm |
| | | 923.7 MHz, Opt3, MCS6[2] | — | -101.1 | -100.0 | dBm |
| | | 923.7 MHz, Opt3, MCS6 | — | -101.1 | -96.5 | dBm |
| | | 923.6 MHz, Opt4, MCS0, header MCS0, with PL = 20 octets | — | -115.8 | — | dBm |
| | | 923.6 MHz, Opt4, MCS2, header MCS2 | — | -113.4 | — | dBm |
| | | 923.6 MHz, Opt4, MCS4[2] | — | -110.3 | -108.2 | dBm |
| | | 923.6 MHz, Opt4, MCS4 | — | -110.3 | -105.4 | dBm |
| | | 923.6 MHz, Opt4, MCS5[2] | — | -107.6 | -106.0 | dBm |
| | | 923.6 MHz, Opt4, MCS5 | — | -107.6 | -102.2 | dBm |
| | | 923.6 MHz, Opt4, MCS6[2] | — | -104.0 | -102.3 | dBm |
| | | 923.6 MHz, Opt4, MCS6 | — | -104.0 | -99.7 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Rx Max Strong Signal Input Level for 10% PER for packet length = 250 octets unless otherwise stated. | $RX_{SAT}$ | 923.5 MHz, Opt2, MCS3 | — | 10 | — | dBm |
| | | 923.5 MHz, Opt2, MCS6 | — | 10 | — | dBm |
| | | 923.7 MHz, Opt3, MCS4 | — | 10 | — | dBm |
| | | 923.7 MHz, Opt3, MCS6 | — | 10 | — | dBm |
| Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 20.5.4 with Desired signal at 3 dB above required sensitivity in Table 20-21, and Undesired signal on an adjacent channel. Requires IR Calibration.[3] | ACR1 | 923.5 MHz, Opt2, MCS3 | — | 33.9 | — | dB |
| | | 923.5 MHz, Opt2, MCS6 | — | 31.8 | — | dB |
| | | 923.7 MHz, Opt3, MCS4 | 33.7 | 35.5 | — | dB |
| | | 923.7 MHz, Opt3, MCS6 | 19.3 | 31.2 | — | dB |
| | | 923.6 MHz, Opt4, MCS4 | — | 32.0 | — | dB |
| | | 923.6 MHz, Opt4, MCS6 | — | 31.1 | — | dB |
| Alternate Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 20.5.5 with Desired signal at 3 dB above required sensitivity in Table 20-21, and Undesired signal at two frequency channels away. Requires IR Calibration.[3] | ACR2 | 923.5 MHz, Opt2, MCS3 | — | 38.9 | — | dB |
| | | 923.5 MHz, Opt2, MCS6 | — | 39.8 | — | dB |
| | | 923.7 MHz, Opt3, MCS4 | 39.8 | 42.9 | — | dB |
| | | 923.7 MHz, Opt3, MCS6 | 35.5 | 38.9 | — | dB |
| | | 923.6 MHz, Opt4, MCS4 | — | 37.0 | — | dB |
| | | 923.6 MHz, Opt4, MCS6 | — | 37.3 | — | dB |
| Image Rejection U/D Ratio for 10% PER. Undesired signal is CW at the RX image frequency. Desired signal is 3dB above required sensitivity level according to IEEE 802.15.4-2020 section 20.5.3. | IR | 923.5 MHz, Opt2, MCS3 | — | 33.9 | — | dB |
| | | 923.5 MHz, Opt2, MCS6 | — | 31.8 | — | dB |
| | | 923.7 MHz, Opt3, MCS4 | — | 35.5 | — | dB |
| | | 923.7 MHz, Opt3, MCS6 | — | 31.2 | — | dB |
| | | 923.6 MHz, Opt4, MCS4 | — | 32.0 | — | dB |
| | | 923.6 MHz, Opt4, MCS6 | — | 31.1 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is modulated and at ± 10 MHz frequency offset.[3] | $BLOCK_{10M}$ | 923.5 MHz, Opt2, MCS3 | — | 59.9 | — | dB |
| | | 923.7 MHz, Opt3, MCS4 | — | 61.3 | — | dB |
| | | 923.7 MHz, Opt3, MCS6 | — | 57.1 | — | dB |
| | | 923.6 MHz, Opt4, MCS4 | — | 63.8 | — | dB |
| | | 923.6 MHz, Opt4, MCS6 | — | 58.1 | — | dB |
| Co-Channel Rejection U/D ratio. Set Desired signal to 3 dB above required sensitivity level according to IEEE 805.15.4-2020 section 20.5.3. Undesired signal level shall be adjusted to make PER = 10%.[3] | CoChR | 923.5 MHz, Opt2, MCS3 | — | -4.1 | — | dB |
| | | 923.5 MHz, Opt2, MCS6 | — | -13.0 | — | dB |
| | | 923.7 MHz, Opt3, MCS4 | -7.4 | -6.5 | — | dB |
| | | 923.7 MHz, Opt3, MCS6 | -14.0 | -13.1 | — | dB |
| | | 923.6 MHz, Opt4, MCS4 | — | -4.9 | — | dB |
| | | 923.6 MHz, Opt4, MCS6 | — | -11.3 | — | dB |
| Rx Energy Detection Magnitude Error, and AGC, averaged over 8 symbols of Short Training Field.[4] | $AGC_{STFME}$ | 923.5 MHz, Opt2, STF | — | 0.8 | — | dB |
| | | 923.7 MHz, Opt3, STF | — | 1.1 | — | dB |
| | | 923.6 MHz, Opt4, STF | — | 0.7 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency Error Sensitivity. Receiver signal level for 10% PER with the desired signal's frequency offset by ± 60 ppm. | $SENS_{FE}$ | 923.5 MHz, Opt2, MCS3 | — | -107.5 | — | dBm |
| | | 923.5 MHz, Opt2, MCS6 | — | -98.4 | — | dBm |
| | | 923.7 MHz, Opt3, MCS4[2] | — | -107.4 | -105.8 | dBm |
| | | 923.7 MHz, Opt3, MCS4 | — | -107.4 | -103.1 | dBm |
| | | 923.7 MHz, Opt3, MCS6[2] | — | -101.0 | -99.4 | dBm |
| | | 923.7 MHz, Opt3, MCS6 | — | -101.0 | -96.5 | dBm |
| | | 923.6 MHz, Opt4, MCS4 | — | -110.1 | — | dBm |
| | | 923.6 MHz, Opt4, MCS6 | — | -104.1 | — | dBm |
| Signal Quality Estimate index [0-255] for the given input signal condition as measured by the receiver with AGC active. | SQE | at SENS Opt3, MCS6 | — | 101 | — | index |
| | | 3 dB above SENS Opt3, MCS6 | — | 121 | — | index |
| | | 10 dB above SENS Opt3, MCS6 | — | 176 | — | index |
| | | at -88 dBm Opt3, MCS6 | — | 197 | — | index |
| | | at -88 dBm and Undesired at ACR1 Opt3, MCS6 | — | 104 | — | index |
| | | at -40 dBm no interferer Opt3, MCS6 | — | 248 | — | index |
| | | at -40 dBm with a co-channel undesired signal level adjusted for 10% PER[3] Opt3, MCS6 | — | 103 | — | index |
| | | at $SENS_{FE}$ Opt3, MCS6, with 60 ppm | — | 99 | — | index |
| Receive Signal Strength Indicator in dB for the given input signal condition as measured by the receiver with AGC active. | RSSI | at SENS Opt3, MCS6[2] | — | -101.2 | — | dBm |
| | | 3 dB above SENS Opt3, MCS6[2] | -100.0 | -98.4 | -96.7 | dBm |
| | | 10 dB above SENS Opt3, MCS6[2] | -93.1 | -91.6 | -89.8 | dBm |
| | | at -88 dBm Opt3, MCS6[2] | -90.1 | -88.4 | -86.6 | dBm |
| | | at -88 dBm and ACR1 Opt3, MCS6[2] | -89.7 | -88.1 | -86.8 | dBm |
| | | at -40 dBm no interferer Opt3, MCS6[2] | -42.8 | -40.8 | -38.6 | dBm |
| | | at -40 dBm with a co-channel undesired signal level adjusted for 10% PER[3] Opt3, MCS6[2] | -42.4 | -40.8 | -39.1 | dBm |
| | | at $SENS_{FE}$ Opt3, MCS6, with 60 ppm[2] | -103.0 | -101.3 | -100.0 | dBm |

**Note:**

1. Typical frequency is defined in the Test Condition column, and varies on selected Option.
2. Min/Max numbers are measured at typical voltage, at typical $F_{RANGE}$ frequency, and at $T_A$ = 25 °C.
3. The undesired signal shall use the same modulation type and settings as the desired signal being tested, but containing different pseudo random data in its PSDU. STF and LTF are excluded from the frame of the undesired signal.
4. Using a Short Training Field signal (section 20.2.2 of IEEE 802.15.4-2020), sweep Antenna input level in 2 dB steps starting from 10 dB above required sensitivity to 50 dB above required sensitivity of the Option in test with MCS0 in 802.15.4-2020 Table 20-21. At each 2 dB step, record the input signal level at the 50 Ω Antenna port along with the signal level measured by the receiver averaged over 8 STF symbols. The Magnitude Error is the absolute value of the difference between these two at the 2 dB step with the worst Error. AGC_STFME = Max( |Avg(Rx_meas) - Rx_applied| ).

#### 4.9.6.2 914 MHz Band RF SUN OFDM Receiver Characteristics

**Table 4.32. 914 MHz Band RF SUN OFDM Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | 914 | 928 | MHz |
| Rx Sensitivity for 10% Packet Error Rate (PER) with no interferer | SENS | Opt1, MCS0[1] | — | -110.8 | -109.6 | dBm |
| | | Opt1, MCS0 | — | -110.8 | -106.0 | dBm |
| | | Opt1, MCS1 | — | -109.7 | — | dBm |
| | | Opt1, MCS2[1] | — | -107.1 | -106.1 | dBm |
| | | Opt1, MCS2 | — | -107.1 | -102.7 | dBm |
| | | Opt1, MCS3 | — | -104.3 | — | dBm |
| | | Opt1, MCS4 | — | -101.8 | — | dBm |
| | | Opt1, MCS5 | — | -99.0 | — | dBm |
| | | Opt1, MCS6[1] | — | -95.3 | -94.6 | dBm |
| | | Opt1, MCS6 | — | -95.3 | -91.0 | dBm |
| | | Opt2, MCS0 | — | -113.0 | — | dBm |
| | | Opt2, MCS1 | — | -112.2 | — | dBm |
| | | Opt2, MCS2 | — | -109.9 | — | dBm |
| | | Opt2, MCS3[1] | — | -107.4 | -106.1 | dBm |
| | | Opt2, MCS3 | — | -107.4 | -102.4 | dBm |
| | | Opt2, MCS4 | — | -104.9 | — | dBm |
| | | Opt2, MCS5 | — | -102.1 | — | dBm |
| | | Opt2, MCS6[1] | — | -98.5 | -97.3 | dBm |
| | | Opt2, MCS6 | — | -98.5 | -94.3 | dBm |
| | | Opt3, MCS1, header MCS1 | — | -114.3 | — | dBm |
| | | Opt3, MCS4 | — | -107.7 | — | dBm |
| | | Opt3, MCS6[1] | — | -101.1 | -100.1 | dBm |
| | | Opt3, MCS6 | — | -101.1 | -96.5 | dBm |
| | | Opt4, MCS0, header MCS0, with PL = 20 octets | — | -116.0 | — | dBm |
| | | Opt4, MCS6[1] | — | -104.0 | -102.6 | dBm |
| | | Opt4, MCS6 | — | -104.0 | -99.7 | dBm |
| Rx Max Strong Signal Input Level for 10% PER for packet length = 250 octets unless otherwise stated. | $RX_{SAT}$ | Opt1, MCS2 | — | 10 | — | dBm |
| | | Opt1, MCS6 | — | 10 | — | dBm |
| | | Opt2, MCS3 | — | 10 | — | dBm |
| | | Opt2, MCS6 | — | 10 | — | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 20.5.4 with Desired signal at 3 dB above required sensitivity in Table 20-21, and Undesired signal on an adjacent channel. Requires IR Calibration.[2] | ACR1 | Opt1, MCS2 | — | 30.2 | — | dB |
| | | Opt1, MCS6 | — | 27.8 | — | dB |
| | | Opt2, MCS3 | — | 33.9 | — | dB |
| | | Opt2, MCS6 | — | 34.7 | — | dB |
| Alternate Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 20.5.5 with Desired signal at 3 dB above required sensitivity in Table 20-21, and Undesired signal at two frequency channels away. Requires IR Calibration.[2] | ACR2 | Opt1, MCS2 | — | 41.0 | — | dB |
| | | Opt1, MCS6 | — | 36.6 | — | dB |
| | | Opt2, MCS3 | — | 38.9 | — | dB |
| | | Opt2, MCS6 | — | 39.7 | — | dB |
| Image Rejection U/D Ratio for 10% PER. Undesired signal is CW at the RX image frequency. Desired signal is 3dB above required sensitivity level according to IEEE 802.15.4-2020 section 20.5.3. | IR | Opt1, MCS2 | — | 30.2 | — | dB |
| | | Opt1, MCS6 | — | 27.8 | — | dB |
| | | Opt2, MCS3 | — | 33.9 | — | dB |
| | | Opt2, MCS6 | — | 34.7 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is modulated and at ± 10 MHz frequency offset.[2] | $BLOCK_{10M}$ | Opt1, MCS2 | — | 54.5 | — | dB |
| | | Opt1, MCS6 | — | 48.4 | — | dB |
| | | Opt2, MCS3 | — | 60.2 | — | dB |
| | | Opt2, MCS6 | — | 52.2 | — | dB |
| Co-Channel Rejection U/D ratio. Set Desired signal to 3 dB above required sensitivity level according to IEEE 805.15.4-2020 section 20.5.3. Undesired signal level shall be adjusted to make PER = 10%.[2] | CoChR | Opt1, MCS2 | — | -2.1 | — | dB |
| | | Opt1, MCS6 | — | -14.0 | — | dB |
| | | Opt2, MCS3 | — | -4.0 | — | dB |
| | | Opt2, MCS6 | — | -13.0 | — | dB |
| Rx Energy Detection Magnitude Error, and AGC, averaged over 8 symbols of Short Training Field.[3] | $AGC_{STFME}$ | Opt1, STF | — | 0.7 | — | dB |
| | | Opt2, STF | — | 0.6 | — | dB |
| | | Opt3, STF | — | 0.8 | — | dB |
| | | Opt4, STF | — | 0.5 | — | dB |
| Frequency Error Sensitivity. Receiver signal level for 10% PER with the desired signal's frequency offset by ± 60 ppm. | $SENS_{FE}$ | Opt1, MCS2 | — | -107.1 | — | dBm |
| | | Opt1, MCS6 | — | -95.3 | — | dBm |
| | | Opt2, MCS3 | — | -107.6 | — | dBm |
| | | Opt2, MCS6 | — | -98.4 | — | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal Quality Estimate index [0-255] for the given input signal condition as measured by the receiver with AGC active. | SQE | at SENS Opt1, MCS6 | — | 100 | — | index |
| | | 3 dB above SENS Opt1, MCS6 | — | 120 | — | index |
| | | 10 dB above SENS Opt1, MCS6 | — | 173 | — | index |
| | | at -82 dBm Opt1, MCS6 | — | 194 | — | index |
| | | at -82 dBm and Undesired at ACR1 Opt1, MCS6 | — | 102 | — | index |
| | | at -40 dBm no interferer Opt1, MCS6 | — | 254 | — | index |
| | | at -40 dBm with a co-channel undesired signal level adjusted for 10% PER[2] Opt1, MCS6 | — | 98 | — | index |
| | | at $SENS_{FE}$ Opt1, MCS6, with 60 ppm | — | 97 | — | index |
| Receive Signal Strength Indicator in dB for the given input signal condition as measured by the receiver with AGC active. | RSSI | at SENS Opt1, MCS6 | — | -94.1 | — | dBm |
| | | 3 dB above SENS Opt1, MCS6 | — | -91.1 | — | dBm |
| | | 10 dB above SENS Opt1, MCS6 | — | -84.2 | — | dBm |
| | | at -82 dBm, Opt1, MCS6 | — | -81.2 | — | dBm |
| | | at -82 dBm and ACR1 Opt1, MCS6 | — | -81.0 | — | dBm |
| | | at -40 dBm no interferer Opt1, MCS6 | — | -39.5 | — | dBm |
| | | at -40 dBm with a co-channel undesired signal level adjusted for 10% PER[2] Opt1, MCS6 | — | -39.6 | — | dBm |
| | | at $SENS_{FE}$ Opt1, MCS6, with 60 ppm | — | -94.3 | — | dBm |

**Note:**

1. Min/Max numbers are measured at typical voltage, at typical $F_{RANGE}$ frequency, and at $T_A$ = 25 °C.
2. The undesired signal shall use the same modulation type and settings as the desired signal being tested, but containing different pseudo random data in its PSDU. STF and LTF are excluded from the frame of the undesired signal.
3. Using a Short Training Field signal (section 20.2.2 of IEEE 802.15.4-2020), sweep Antenna input level in 2 dB steps starting from 10 dB above required sensitivity to 50 dB above required sensitivity of the Option in test with MCS0 in 802.15.4-2020 Table 20-21. At each 2 dB step, record the input signal level at the 50 Ω Antenna port along with the signal level measured by the receiver averaged over 8 STF symbols. The Magnitude Error is the absolute value of the difference between these two at the 2 dB step with the worst Error. AGC_STFME = Max( |Avg(Rx_meas) - Rx_applied| ).

#### 4.9.6.3 866 MHz Band RF SUN OFDM Receiver Characteristics

**Table 4.33. 866 MHz Band RF SUN OFDM Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 863.1 | 866.5 | 876 | MHz |
| Rx Sensitivity for 10% Packet Error Rate (PER) with no interferer | SENS | Opt4, MCS0, header MCS0, with PL = 20 octets | — | -115.6 | — | dBm |
| | | Opt4, MCS2, header MCS2[1] | — | -113.2 | -110.4 | dBm |
| | | Opt4, MCS2, header MCS2 | — | -113.2 | -108.9 | dBm |
| | | Opt4, MCS4[1] | — | -110.1 | -108.1 | dBm |
| | | Opt4, MCS4 | — | -110.1 | -105.1 | dBm |
| | | Opt4, MCS5 | — | -107.4 | — | dBm |
| | | Opt4, MCS6[1] | — | -103.8 | -102.1 | dBm |
| | | Opt4, MCS6 | — | -103.8 | -99.9 | dBm |
| Rx Max Strong Signal Input Level for 10% PER for packet length = 250 octets unless otherwise stated. | $RX_{SAT}$ | Opt4, MCS4 | — | 10 | — | dBm |
| | | Opt4, MCS6 | — | 10 | — | dBm |
| Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 20.5.4 with Desired signal at 3 dB above required sensitivity in Table 20-21, and Undesired signal on an adjacent channel. Requires IR Calibration.[2] | ACR1 | Opt4, MCS4 | — | 34.8 | — | dB |
| | | Opt4, MCS6 | — | 32.5 | — | dB |
| Alternate Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 20.5.5 with Desired signal at 3 dB above required sensitivity in Table 20-21, and Undesired signal at two frequency channels away. Requires IR Calibration.[2] | ACR2 | Opt4, MCS4 | — | 40.2 | — | dB |
| | | Opt4, MCS6 | — | 37.7 | — | dB |
| Image Rejection U/D Ratio for 10% PER. Undesired signal is CW at the RX image frequency. Desired signal is 3dB above required sensitivity level according to IEEE 802.15.4-2020 section 20.5.3. | IR | Opt4, MCS4 | — | 34.8 | — | dB |
| | | Opt4, MCS6 | — | 32.5 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is modulated and at ± 10 MHz frequency offset.[2] | $BLOCK_{10M}$ | Opt4, MCS4 | — | 64.4 | — | dB |
| | | Opt4, MCS6 | — | 58.3 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Co-Channel Rejection U/D ratio. Set Desired signal to 3 dB above required sensitivity level according to IEEE 805.15.4-2020 section 20.5.3. Undesired signal level shall be adjusted to make PER = 10%.[2] | CoChR | Opt4, MCS4 | — | -4.9 | — | dB |
| | | Opt4, MCS6 | — | -11.3 | — | dB |
| Rx Energy Detection Magnitude Error, and AGC, averaged over 8 symbols of Short Training Field.[3] | $AGC_{STFME}$ | Opt4, STF | — | 3.9 | — | dB |
| Frequency Error Sensitivity. Receiver signal level for 10% PER with the desired signal's frequency offset by ± 60 ppm. | $SENS_{FE}$ | Opt4, MCS4 | — | -109.9 | — | dBm |
| | | Opt4, MCS6 | — | -102.7 | — | dBm |
| Signal Quality Estimate index [0-255] for the given input signal condition as measured by the receiver with AGC active. | SQE | at SENS Opt4, MCS6 | — | 103 | — | index |
| | | 3 dB above SENS Opt4, MCS6 | — | 124 | — | index |
| | | 10 dB above SENS Opt4, MCS6 | — | 172 | — | index |
| | | at -91 dBm, Opt4, MCS6 | — | 182 | — | index |
| | | at -91 dBm and ACR1 Opt4, MCS6 | — | 122 | — | index |
| | | at -40 dBm no interferer Opt4, MCS6 | — | 214 | — | index |
| | | at -40 dBm with a co-channel undesired signal level adjusted for 10% PER[2] Opt4, MCS6 | — | 104 | — | index |
| | | at $SENS_{FE}$ Opt4, MCS6, with 60 ppm | — | 99 | — | index |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Receive Signal Strength Indicator in dB for the given input signal condition as measured by the receiver with AGC active. | RSSI | at SENS Opt4, MCS6 | — | -104.3 | — | dBm |
| | | 3 dB above SENS Opt4, MCS6 | — | -101.4 | — | dBm |
| | | 10 dB above SENS Opt4, MCS6 | — | -94.4 | — | dBm |
| | | at -91 dBm Opt4, MCS6 | — | -92.5 | — | dBm |
| | | at -91 dBm and Undesired at ACR1 Opt4, MCS6 | — | -92.2 | — | dBm |
| | | at -40 dBm no interferer Opt4, MCS6 | — | -43.1 | — | dBm |
| | | at -40 dBm with a co-channel undesired signal level adjusted for 10% PER[2] Opt4, MCS6 | — | -42.5 | — | dBm |
| | | at $SENS_{FE}$ Opt4, MCS6, with 60 ppm | — | -105.0 | — | dBm |

**Note:**

1. Min/Max numbers are measured at typical voltage, at typical $F_{RANGE}$ frequency, and at $T_A$ = 25 °C.
2. The undesired signal shall use the same modulation type and settings as the desired signal being tested, but containing different pseudo random data in its PSDU. STF and LTF are excluded from the frame of the undesired signal.
3. Using a Short Training Field signal (section 20.2.2 of IEEE 802.15.4-2020), sweep Antenna input level in 2 dB steps starting from 10 dB above required sensitivity to 50 dB above required sensitivity of the Option in test with MCS0 in 802.15.4-2020 Table 20-21. At each 2 dB step, record the input signal level at the 50 Ω Antenna port along with the signal level measured by the receiver averaged over 8 STF symbols. The Magnitude Error is the absolute value of the difference between these two at the 2 dB step with the worst Error. AGC_STFME = Max( |Avg(Rx_meas) - Rx_applied| ).

#### 4.9.6.4 490 MHz Band RF SUN OFDM Receiver Characteristics

**Table 4.34. 490 MHz Band RF SUN OFDM Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 470 | 490 | 510 | MHz |
| Rx Sensitivity for 10% Packet Error Rate (PER) with no interferer | SENS | Opt4, MCS0, header MCS0, with PL = 20 octets | — | -116.8 | — | dBm |
| | | Opt4, MCS2, header MCS2 | — | -114.5 | — | dBm |
| | | Opt4, MCS4, header MCS2 | — | -111.4 | — | dBm |
| | | Opt4, MCS5, header MCS2 | — | -108.7 | — | dBm |
| | | Opt4, MCS6, header MCS2 | — | -105.2 | — | dBm |
| Rx Max Strong Signal Input Level for 10% PER for packet length = 250 octets unless otherwise stated. | $RX_{SAT}$ | Opt4, MCS2, header MCS2, with PL = 20 octets | — | 10 | — | dBm |
| | | Opt4, MCS6, header MCS2 | — | 10 | — | dBm |
| Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 20.5.4 with Desired signal at 3 dB above required sensitivity in Table 20-21, and Undesired signal on an adjacent channel. Requires IR Calibration.[1] | ACR1 | Opt4, MCS2, header MCS2 | — | 43.9 | — | dB |
| | | Opt4, MCS6, header MCS2 | — | 34.0 | — | dB |
| Alternate Adjacent Channel Rejection U/D ratio for 10% PER according to IEEE 802.15.4-2020 section 20.5.5 with Desired signal at 3 dB above required sensitivity in Table 20-21, and Undesired signal at two frequency channels away. Requires IR Calibration.[1] | ACR2 | Opt4, MCS2, header MCS2 | — | 47.8 | — | dB |
| | | Opt4, MCS6, header MCS2 | — | 37.5 | — | dB |
| Image Rejection U/D Ratio for 10% PER. Undesired signal is CW at the RX image frequency. Desired signal is 3dB above required sensitivity level according to IEEE 802.15.4-2020 section 20.5.3. | IR | Opt4, MCS2, header MCS2 | — | 43.9 | — | dB |
| | | Opt4, MCS6, header MCS2 | — | 34.0 | — | dB |
| Blocking Selectivity U/D ratio for 10% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is modulated and at ± 10 MHz frequency offset.[1] | $BLOCK_{10M}$ | Opt4, MCS2, header MCS2 | — | 69.0 | — | dB |
| | | Opt4, MCS6, header MCS2 | — | 59.8 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Co-Channel Rejection U/D ratio. Set Desired signal to 3 dB above required sensitivity level according to IEEE 805.15.4-2020 section 20.5.3. Undesired signal level shall be adjusted to make PER = 10%.[1] | CoChR | Opt4, MCS2, header MCS2 | — | -2.2 | — | dB |
| | | Opt4, MCS6, header MCS2 | — | -11.4 | — | dB |
| Rx Energy Detection Magnitude Error, and AGC, averaged over 8 symbols of Short Training Field.[2] | $AGC_{STFME}$ | Opt4, STF | — | 0.5 | — | dB |
| Frequency Error Sensitivity. Receiver signal level for 10% PER with the desired signal's frequency offset by ± 60 ppm. | $SENS_{FE}$ | Opt4, MCS2, header MCS2 | — | -114.0 | — | dBm |
| | | Opt4, MCS6, header MCS2 | — | -105.0 | — | dBm |
| Signal Quality Estimate index [0-255] for the given input signal condition as measured by the receiver with AGC active. | SQE | at SENS Opt4, MCS6 | — | 99 | — | index |
| | | 3 dB above SENS Opt4, MCS6 | — | 119 | — | index |
| | | 10 dB above SENS Opt4, MCS6 | — | 166 | — | index |
| | | at -91 dBm, Opt4, MCS6 | — | 187 | — | index |
| | | at -91 dBm and ACR1 Opt4, MCS6 | — | 102 | — | index |
| | | at -40 dBm no interferer Opt4, MCS6 | — | 216 | — | index |
| | | at -40 dBm with a co-channel undesired signal level adjusted for 10% PER[1] Opt4, MCS6 | — | 104 | — | index |
| | | at $SENS_{FE}$ Opt4, MCS6, with 60 ppm | — | 99 | — | index |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Receive Signal Strength Indicator in dB for the given input signal condition as measured by the receiver with AGC active. | RSSI | at SENS Opt4, MCS6 | — | -107.1 | — | dBm |
| | | 3 dB above SENS Opt4, MCS6 | — | -104.3 | — | dBm |
| | | 10 dB above SENS Opt4, MCS6 | — | -97.4 | — | dBm |
| | | at -91 dBm Opt4, MCS6 | — | -93.4 | — | dBm |
| | | at -91 dBm and Undesired at ACR1 Opt4, MCS6 | — | -92.4 | — | dBm |
| | | at -40 dBm no interferer Opt4, MCS6 | — | -44.5 | — | dBm |
| | | at -40 dBm with a co-channel undesired signal level adjusted for 10% PER[1] Opt4, MCS6 | — | -44.2 | — | dBm |
| | | at $SENS_{FE}$ Opt4, MCS6, with 60 ppm | — | -106.8 | — | dBm |

**Note:**

1. The undesired signal shall use the same modulation type and settings as the desired signal being tested, but containing different pseudo random data in its PSDU. STF and LTF are excluded from the frame of the undesired signal.
2. Using a Short Training Field signal (section 20.2.2 of IEEE 802.15.4-2020), sweep Antenna input level in 2 dB steps starting from 10 dB above required sensitivity to 50 dB above required sensitivity of the Option in test with MCS0 in 802.15.4-2020 Table 20-21. At each 2 dB step, record the input signal level at the 50 Ω Antenna port along with the signal level measured by the receiver averaged over 8 STF symbols. The Magnitude Error is the absolute value of the difference between these two at the 2 dB step with the worst Error. AGC_STFME = Max( |Avg(Rx_meas) - Rx_applied| ).

## 4.10 Oscillators

### 4.10.1 High Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = IOVDD0-2 = 3.6 V. DC-DC not used. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

**Table 4.35. High Frequency Crystal Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal Frequency | $F_{HFXO}$ | see note [1] | 38.0 | 39.0 | 40.0 | MHz |
| Supported crystal equivalent series resistance (ESR) | $ESR_{HFXO}$ | 39.0 MHz, $C_L$ = 10 pF[2] | — | — | 60 | Ω |
| Supported range of crystal load capacitance[3] | $C_{HFXO\_LC}$ | 39.0 MHz, ESR = 40 Ohm[4] | — | 10 | — | pF |
| Supply Current | $I_{HFXO}$ | | — | 479 | — | µA |
| Startup Time[5] | $T_{STARTUP}$ | 39.0 MHz, ESR = 40 Ω, $C_L$ = 10 pF | — | 201 | — | µs |
| On-chip tuning cap step size[6] | $SS_{HFXO}$ | | — | 0.04 | — | pF |
| HFCLKOUT load capacitance | $C_{HFCLKOUT}$ | | — | 20 | 30 | pF |
| HFCLKOUT output voltage | $V_{HFCLKOUT}$ | | 0 | — | 1.2 | V |
| HFCLKOUT AC output amplitude, XOUTBIASANA = 5, $C_{HFCLKOUT}$ = 20 pF | $VAC_{HFCLKOUT}$ | XOUTCFANA = 0 | — | 470 | — | mVpp |
| | | XOUTCFANA = 1 | — | 510 | — | mVpp |
| | | XOUTCFANA = 2 | — | 560 | — | mVpp |
| | | XOUTCFANA = 3 | — | 615 | — | mVpp |
| HFCLKOUT current consumption | $I_{HFCLKOUT}$ | $C_{HFCLKOUT}$ ≤ 10 pF, XOUTBIASANA = 3 | — | 3.1 | — | mA |
| | | 10 pF < $C_{HFCLKOUT}$ ≤ 20 pF, XOUTBIASANA = 5 | — | 3.9 | — | mA |
| | | 20 pF < $C_{HFCLKOUT}$ ≤ 30 pF, XOUTBIASANA = 15 | — | 6.3 | — | mA |
| Frequency shift of HFXTAL when HFCLKOUT is active | $FS_{HFCLKOUT}$ | Assuming crystal pullability of 13 ppm/pF | -1.5 | — | 4.5 | ppm |
| HFCLKOUT shorting output resistance | $RS_{HFCLKOUT}$ | When output is disabled | — | 137 | — | Ω |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Total harmonic distortion, XOUTBIASANA = 5, $C_{HFCLKOUT}$ = 20 pF | $THD_{HFCLKOUT}$ | XOUTCFANA = 0 | — | 8.53 | — | % |
| | | XOUTCFANA = 1 | — | 10.05 | — | % |
| | | XOUTCFANA = 2 | — | 11.98 | — | % |
| | | XOUTCFANA = 3 | — | 14.39 | — | % |

**Note:**

1. All sub-GHz RF measurements made using a 39 MHz crystal. Other crystal frequencies supported, but RF performance may vary.
2. The crystal should have a maximum ESR less than or equal to this maximum rating.
3. Total load capacitance as seen by the crystal.
4. It is recommended to use a crystal with a 10 pF load capacitance rating. Only crystals with a 10 pF load cap rating have been characterized for RF use.
5. Startup time does not include time implemented by programmable TIMEOUTSTEADY delay.
6. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for the each of the individual tuning capacitors is twice this value.

### 4.10.2 Low Frequency Crystal Oscillator

**Table 4.36. Low Frequency Crystal Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal frequency | $F_{LFXO}$ | | — | 32.768 | — | kHz |
| Supported crystal equivalent series resistance (ESR) | $ESR_{LFXO}$ | GAIN = 0 | — | — | 80 | kΩ |
| | | GAIN = 1 to 3 | — | — | 100 | kΩ |
| Supported range of crystal load capacitance [1] | $C_{L\_LFXO}$ | GAIN = 0 | 4 | — | 6 | pF |
| | | GAIN = 1 | 6 | — | 10 | pF |
| | | GAIN = 2 (see note[2]) | 10 | — | 12.5 | pF |
| | | GAIN = 3 (see note[2]) | 12.5 | — | 18 | pF |
| Current consumption | $I_{CL12p5}$ | ESR = 70 kΩ, $C_L$ = 12.5 pF, GAIN[3] = 2, AGC[4] = 1 | — | 295 | — | nA |
| Startup time | $T_{STARTUP}$ | ESR = 70 kΩ, $C_L$ = 7 pF, GAIN[3] = 1, AGC[4] = 1 | — | 49 | — | ms |
| On-chip tuning cap step size | $SS_{LFXO}$ | | — | 0.26 | — | pF |
| On-chip tuning capacitor value at minimum setting[5] | $C_{LFXO\_MIN}$ | CAPTUNE = 0 | — | 7 | — | pF |
| On-chip tuning capacitor value at maximum setting[5] | $C_{LFXO\_MAX}$ | CAPTUNE = 0x4F | — | 27.7 | — | pF |

**Note:**

1. Total load capacitance seen by the crystal.
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register.
4. In LFXO_CFG Register.
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

### 4.10.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = IOVDD0-2 = 3.6 V. DC-DC not used. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

**Table 4.37. High Frequency RC Oscillator (HFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency Accuracy | $F_{HFRCO\_ACC}$ | For all production calibrated frequencies | -3 | — | 3 | % |
| Current consumption on all supplies[1] [2] | $I_{HFRCO}$ | $F_{HFRCO}$ = 4 MHz | — | 43 | — | µA |
| | | $F_{HFRCO}$ = 5 MHz [3] | — | 40 | — | µA |
| | | $F_{HFRCO}$ = 7 MHz | — | 75 | — | µA |
| | | $F_{HFRCO}$ = 10 MHz [3] | — | 77 | — | µA |
| | | $F_{HFRCO}$ = 13 MHz | — | 94 | — | µA |
| | | $F_{HFRCO}$ = 16 MHz | — | 103 | — | µA |
| | | $F_{HFRCO}$ = 19 MHz | — | 107 | — | µA |
| | | $F_{HFRCO}$ = 20 MHz [3] | — | 115 | — | µA |
| | | $F_{HFRCO}$ = 26 MHz | — | 132 | — | µA |
| | | $F_{HFRCO}$ = 32 MHz | — | 155 | — | µA |
| | | $F_{HFRCO}$ = 38 MHz [4] | — | 187 | — | µA |
| | | $F_{HFRCO}$ = 40 MHz [3] | — | 185 | — | µA |
| | | $F_{HFRCO}$ = 48 MHz [4] | — | 224 | — | µA |
| | | $F_{HFRCO}$ = 56 MHz [4] | — | 246 | — | µA |
| | | $F_{HFRCO}$ = 64 MHz [4] | — | 286 | — | µA |
| | | $F_{HFRCO}$ = 80 MHz [4] | — | 303 | — | µA |
| Clock Out current for HFRCODPLL[2] [5] | $I_{CLKOUT\_HFRCODPLL}$ | FORCEEN bit of HFRCO0_CTRL = 1 | — | 2.5 | — | µA/MHz |
| Clock Out current for HFRCOEM23[2] [5] | $I_{CLKOUT\_HFRCOEM23}$ | FORCEEN bit of HFRCOEM23_CTRL = 1 | — | 1.0 | — | µA/MHz |
| Startup time[6] | $T_{STARTUP}$ | FREQRANGE = 0 to 7 | — | 0.968 | — | µs |
| | | FREQRANGE = 8 to 15 | — | 0.6 | — | µs |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Band frequency limits[7] | $f_{HFRCO\_BAND}$ | FREQRANGE = 0 | 3.71 | — | 5.24 | MHz |
| | | FREQRANGE = 1 | 4.39 | — | 6.26 | MHz |
| | | FREQRANGE = 2 | 5.25 | — | 7.55 | MHz |
| | | FREQRANGE = 3 | 6.22 | — | 9.01 | MHz |
| | | FREQRANGE = 4 | 7.88 | — | 11.6 | MHz |
| | | FREQRANGE = 5 | 9.90 | — | 14.6 | MHz |
| | | FREQRANGE = 6 | 11.5 | — | 17.0 | MHz |
| | | FREQRANGE = 7 | 14.1 | — | 20.9 | MHz |
| | | FREQRANGE = 8 | 16.4 | — | 24.7 | MHz |
| | | FREQRANGE = 9 | 19.8 | — | 30.4 | MHz |
| | | FREQRANGE = 10 | 22.7 | — | 34.9 | MHz |
| | | FREQRANGE = 11 | 28.6 | — | 44.4 | MHz |
| | | FREQRANGE = 12 | 33.0 | — | 51.0 | MHz |
| | | FREQRANGE = 13 | 42.2 | — | 64.6 | MHz |
| | | FREQRANGE = 14 | 48.8 | — | 74.8 | MHz |
| | | FREQRANGE = 15 | 57.6 | — | 87.4 | MHz |

**Note:**

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. When HFRCO is activated the FSRCO is also activated. This prevents direct measurement of only the HFRCO current. The specified current for HFRCO does not include the FSRCO current which is typically 41 µA.
3. This frequency is calibrated for the HFRCOEM23 only.
4. This frequency is calibrated for the HFRCODPLL (HFRCO0) only.
5. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
6. Hardware delay ensures settling to within ± 0.5%. Hardware also enforces this delay on a band change.
7. The frequency band limits represent the lowest and highest frequency which each band can achieve over the operating range.

### 4.10.4 Fast Start_Up RC Oscillator (FSRCO)

**Table 4.38. Fast Start_Up RC Oscillator (FSRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FSRCO frequency | $F_{FSRCO}$ | | 17.2 | 20 | 21.2 | MHz |

### 4.10.5 Low Frequency RC Oscillator (LFRCO)

**Table 4.39. Low Frequency RC Oscillator (LFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Nominal oscillation frequency | $F_{LFRCO}$ | | — | 32.768 | — | kHz |
| Frequency accuracy | $F_{LFRCO\_ACC}$ | | -3 | — | 3 | % |
| Frequency calibration step | $F_{TRIM\_STEP}$ | Typical trim step at mid-scale | — | 0.33 | — | % |
| Startup time | $t_{STARTUP}$ | | — | 182 | — | µs |
| Current consumption | $I_{LFRCO}$ | | — | 191 | — | nA |

### 4.10.6 Ultra Low Frequency RC Oscillator

**Table 4.40. Ultra Low Frequency RC Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $F_{ULFRCO}$ | | 0.944 | 1.0 | 1.095 | kHz |

### 4.11 GPIO Pins (3 V GPIO pins)

**Table 4.41. GPIO Pins (3 V GPIO pins)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Leakage current | $I_{LEAK\_IO}$ | MODEx = DISABLED, IOVDD = 1.71 V | — | 1.9 | — | nA |
| | | MODEx = DISABLED, IOVDD = 3.6 V | — | 2.5 | — | nA |
| | | MODEx = DISABLED, IOVDD = 3.8 V, $T_A$ = 125 °C, Pins PA00, PB00-PB01, PC09-PC10, and PD06-PD07 | — | — | 250 | nA |
| | | MODEx = DISABLED, IOVDD = 3.8 V, $T_A$ = 125 °C, all other GPIO | — | — | 200 | nA |
| Input low voltage[1] | $V_{IL}$ | Any GPIO pin | — | — | 0.3 * IOVDD | V |
| | | RESETn | — | — | 0.3 * DVDD | V |
| Input high voltage[1] | $V_{IH}$ | Any GPIO pin | 0.7 * IOVDD | — | — | V |
| | | RESETn | 0.7 * DVDD | — | — | V |
| Hysteresis of input voltage | $V_{HYS}$ | Any GPIO pin | 0.05 * IOVDD | — | — | V |
| | | RESETn | 0.05 * DVDD | — | — | V |
| Output high voltage | $V_{OH}$ | Sourcing 20 mA, IOVDD = 3.6 V | 0.8 * IOVDD | — | — | V |
| | | Sourcing 8 mA, IOVDD = 1.71 V | 0.6 * IOVDD | — | — | V |
| Output low voltage | $V_{OL}$ | Sinking 20 mA, IOVDD = 3.6 V | — | — | 0.2 * IOVDD | V |
| | | Sinking 8 mA, IOVDD = 1.71 V | — | — | 0.4 * IOVDD | V |
| GPIO rise time | $T_{GPIO\_RISE}$ | IOVDD = 3.6 V, $C_{load}$ = 50 pF, SLEWRATE = 4, 10% to 90% | — | 8.4 | — | ns |
| | | IOVDD = 1.71 V, $C_{load}$ = 50 pF, SLEWRATE = 4, 10% to 90% | — | 13 | — | ns |
| GPIO fall time | $T_{GPIO\_FALL}$ | IOVDD = 3.6 V, $C_{load}$ = 50 pF, SLEWRATE = 4, 90% to 10% | — | 7.1 | — | ns |
| | | IOVDD = 1.71 V, $C_{load}$ = 50 pF, SLEWRATE = 4, 90% to 10% | — | 11.9 | — | ns |
| Pull up/down resistance[2] | $R_{PULL}$ | Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT = 1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0. | 35 | 42 | 55 | kΩ |
| | | RESETn pin. Pull-up to DVDD | 35 | 42 | 55 | kΩ |
| Maximum filtered glitch width | $T_{GF}$ | MODE = INPUT, DOUT = 1 | — | 27 | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RESETn low time to ensure pin reset | $T_{RESET}$ | | 100 | — | — | ns |

**Note:**

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

### 4.12 Analog to Digital Converter (IADC)

Specified at 1 Msps, ADCCLK = 10 MHz, OSR = 2, unless otherwise indicated.

**Table 4.42. Analog to Digital Converter (IADC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Main analog supply | $V_{AVDD}$ | Normal mode | 1.71 | — | 3.8 | V |
| Maximum input range[1] | $V_{IN\_MAX}$ | Maximum allowable input voltage | 0 | — | AVDD | V |
| Full-scale voltage | $V_{FS}$ | Voltage required for full-scale measurement | — | $V_{REF}$ / Gain | — | V |
| Input measurement range | $V_{IN}$ | Differential mode - plus and minus inputs | $-V_{FS}$ | — | $+V_{FS}$ | V |
| | | Single-ended mode - one input tied to ground | 0 | — | $V_{FS}$ | V |
| Input sampling capacitance | Cs | Analog Gain = 1x | — | 1.8 | — | pF |
| | | Analog Gain = 2x | — | 3.6 | — | pF |
| | | Analog Gain = 3x | — | 5.4 | — | pF |
| | | Analog Gain = 4x | — | 7.2 | — | pF |
| | | Analog Gain = 0.5x | — | 0.9 | — | pF |
| ADC clock frequency | $f_{ADC\_CLK}$ | Normal mode, Gain = 1x or 0.5x | — | — | 10 | MHz |
| | | Normal mode, Gain = 2x | — | — | 5 | MHz |
| | | Normal mode, Gain = 3x or 4x | — | — | 2.5 | MHz |
| Input sampling frequency | $f_S$ | Normal mode | — | $f_{ADC\_CLK}/4$ | — | MHz |
| Throughput rate | $f_{SAMPLE}$ | Normal mode, $f_{ADC\_CLK}$ = 10 MHz, OSR = 2 | — | — | 1 | Msps |
| | | Normal mode, $f_{ADC\_CLK}$ = 10 MHz, OSR = 32 | — | — | 76.9 | ksps |
| Current from all supplies, continuous operation | $I_{ADC\_CONT}$ | Normal mode, 1 Msps, OSR = 2, $f_{ADC\_CLK}$ = 10 MHz | — | 305 | 385 | µA |
| Current in standby mode. ADC is not functional but can wake up in 1 µs. | $I_{STBY}$ | Normal mode | — | 14.8 | — | µA |
| ADC startup time | $t_{startup}$ | From power down state | — | 5 | — | µs |
| | | From standby state | — | 1 | — | µs |
| Normal mode ADC resolution[2] | Resolution | OSR = 2 | — | 12 | — | bits |
| | | OSR = 32 | — | 16 | — | bits |
| Differential nonlinearity | DNL | Normal mode. Differential input. OSR = 2 (No missing codes) | -1 | +/- 0.25 | +1.5 | LSB12 |
| Integral nonlinearity | INL | Normal mode. Differential input, OSR = 2 | -2.5 | +/- 0.65 | +2.5 | LSB12 |
| Effective number of bits[3] | ENOB | Normal mode. Differential Input. Gain = 1x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21 V. | 10.7 | 11.7 | — | bits |
| | | Normal mode, Differential input. Gain = 1x, OSR = 32, $f_{IN}$ = 2.5 kHz, Internal VREF = 1.21 V. | — | 13.5 | — | bits |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal to Noise + Distortion Ratio Normal Mode[3] | SNDR | Normal mode. Differential Input. Gain = 1x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21 V | 66 | 72.3 | — | dB |
| | | Normal mode. Differential Input. Gain = 4x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21 V | — | 68.8 | — | dB |
| | | Differential input. Gain = 1x, OSR = 64, $f_{IN}$ = 1.25 kHz, Internal VREF = 1.21 V | — | 83.9 | — | dB |
| Total Harmonic Distortion | THD | Normal mode, Differential input. Gain = 1x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21 V | — | -80.8 | -70 | dB |
| Spurious-Free Dynamic Range | SFDR | Normal mode, Differential input. Gain = 1x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21 V | 72 | 86.5 | — | dB |
| Common Mode Rejection Ratio | CMRR | Normal mode. DC to 100 Hz | — | 87.0 | — | dB |
| | | Normal mode. AC high frequency. | — | 68.6 | — | dB |
| Power Supply Rejection Ratio | PSRR | Normal mode. DC to 100 Hz | — | 80.4 | — | dB |
| | | Normal mode. AC high frequency, using internal VBGR | — | 33.4 | — | dB |
| | | Normal mode. AC high frequency, using VREF pad | — | 65.2 | — | dB |
| External reference voltage range[1] | $V_{EVREF}$ | | 1.0 | — | AVDD | V |
| Offset error, normal mode | OFFSET | Gain = 1x and 0.5x, Differential input | -4.5 | 0.27 | 4.5 | LSB12 |
| | | Gain = 2x, Differential input | -5.5 | 0.27 | 5.5 | LSB12 |
| | | Gain = 3x, Differential input | -5.5 | 0.25 | 5.5 | LSB12 |
| | | Gain = 4x, Differential input | -5.5 | 0.29 | 5.5 | LSB12 |
| Gain error, normal mode | GE | Gain = 1x and 0.5x, using external VREF, $f_{ADC\_CLK}$ = 10 MHz | -0.3 | 0.069 | 0.3 | % |
| | | Gain = 2x, using external VREF, $f_{ADC\_CLK}$ = 5 MHz | -0.4 | 0.151 | 0.4 | % |
| | | Gain = 3x, using external VREF, $f_{ADC\_CLK}$ = 2.5 MHz | -0.7 | 0.186 | 0.7 | % |
| | | Gain = 4x, using external VREF, $f_{ADC\_CLK}$ = 2.5 MHz | -1.1 | 0.227 | 1.1 | % |
| | | Internal VREF [4], all GAIN settings | -1.5 | 0.023 | 1.5 | % |
| Internal reference voltage | $V_{IVREF}$ | | — | 1.21 | — | V |

**Note:**

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.
2. ADC output resolution depends on the OSR and digital averaging settings. With no digital averaging, ADC output resolution is 12 bits at OSR = 2, 13 bits at OSR = 4, 14 bits at OSR = 8, 15 bits at OSR = 16, 16 bits at OSR = 32 and 17 bits at OSR = 64. Digital averaging has a similar impact on ADC output resolution. See the product reference manual for additional details.
3. The relationship between ENOB and SNDR is specified according to the equation: ENOB = (SNDR - 1.76) / 6.02.
4. Includes error from internal VREF drift.

### 4.13 Analog Comparator (ACMP)

**Table 4.43. Analog Comparator (ACMP)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ACMP supply current | $I_{ACMP}$ | BIAS = 2 [1], HYST = DISABLED | — | 675 | — | nA |
| | | BIAS = 3 [1], HYST = DISABLED | — | 2.5 | — | µA |
| | | BIAS = 4, HYST = DISABLED | — | 5.4 | — | µA |
| | | BIAS = 5, HYST = DISABLED | — | 10.7 | — | µA |
| | | BIAS = 6, HYST = DISABLED | — | 26.9 | — | µA |
| | | BIAS = 7, HYST = DISABLED | — | 49.9 | 85 | µA |
| ACMP supply current with hysteresis | $I_{ACMP\_WHYS}$ | BIAS = 2 [1], HYST = SYM30MV | — | 945 | — | nA |
| | | BIAS = 3 [1], HYST = SYM30MV | — | 3.4 | — | µA |
| | | BIAS = 4, HYST = SYM30MV | — | 7.3 | — | µA |
| | | BIAS = 5, HYST = SYM30MV | — | 15.2 | — | µA |
| | | BIAS = 6, HYST = SYM30MV | — | 38.5 | — | µA |
| | | BIAS = 7, HYST = SYM30MV | — | 71.3 | — | µA |
| Current consumption from VREFDIV in continuous mode | $I_{VREFDIV}$ | NEGSEL = VREFDIVAVDD | — | 3.9 | — | µA |
| | | NEGSEL = VREFDIV1V25 | — | 4.4 | — | µA |
| | | NEGSEL = VREFDIV2V5 | — | 7.2 | — | µA |
| Current consumption from VREFDIV in sample/hold mode | $I_{VREFDIV\_SH}$ | NEGSEL = VREFDIV2V5LP | — | 76 | — | nA |
| | | NEGSEL = VREFDIV1V25LP | — | 72 | — | nA |
| | | NEGSEL = VREFDIVAVDDLP | — | 72 | — | nA |
| Current consumption from VSENSEDIV in continuous mode | $I_{VSENSEDIV}$ | NEGSEL = VSENSE01DIV4 | — | 2.0 | — | µA |
| Current consumption from VSENSEDIV in sample/hold mode | $I_{VSENSEDIV\_SH}$ | NEGSEL = VSENSE01DIV4LP | — | 56 | — | nA |
| Hysteresis (BIAS = 2) | $V_{HYST}$ | HYST = SYM10MV[2] | — | 28 | — | mV |
| | | HYST = SYM20MV[2] | — | 52 | — | mV |
| | | HYST = SYM30MV[2] | — | 74 | — | mV |
| Reference voltage | $V_{ACMPREF}$ | Internal 1.25 V Reference | 1.18 | 1.25 | 1.30 | V |
| | | Internal 2.5 V Reference | 2.36 | 2.5 | 2.61 | V |
| Input offset voltage | $V_{OFFSET}$ | BIAS = 2, VCM = 0.15 to AVDD - 0.15 V | -25 | — | 25 | mV |
| | | BIAS = 3, VCM = 0.15 to AVDD - 0.15 V | -25 | — | 25 | mV |
| | | BIAS = 4, VCM = 0.15 to AVDD - 0.15 V | -25 | — | 25 | mV |
| | | BIAS = 7, VCM = 0.15 to AVDD - 0.15 V | -25 | — | 25 | mV |
| Input range | $V_{IN}$ | Input Voltage Range | 0 | — | AVDD | V |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Comparator delay with 100 mV overdrive | $T_{DELAY}$ | BIAS = 2 | — | 1.3 | — | µs |
| | | BIAS = 3 | — | 0.55 | — | µs |
| | | BIAS = 4 | — | 199 | — | ns |
| | | BIAS = 5 | — | 110 | — | ns |
| | | BIAS = 6 | — | 59 | — | ns |
| | | BIAS = 7 | — | 41 | — | ns |
| Capacitive sense oscillator resistance[3] | $R_{CSRESSEL}$ | CSRESSEL = 0 | — | 15 | — | kΩ |
| | | CSRESSEL = 1 | — | 24 | — | kΩ |
| | | CSRESSEL = 2 | — | 42 | — | kΩ |
| | | CSRESSEL = 3 | — | 61 | — | kΩ |
| | | CSRESSEL = 4 | — | 78 | — | kΩ |
| | | CSRESSEL = 5 | — | 96 | — | kΩ |
| | | CSRESSEL = 6 | — | 115 | — | kΩ |

**Note:**

1. When using the 1.25 V or 2.5 V VREF in continuous mode (VREFDIV1V25 or VREFDIV2V5) and BIAS < 4, an additional 1 µA of supply current is required.
2. $V_{CM}$ = 1.25 V
3. Capacitive Sense has been deprecated and is not recommended for use

### 4.14 Digital to Analog Converter (VDAC)

**Table 4.44. Digital to Analog Converter (VDAC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{DACOUT}$ | | 0 | — | VREF | V |
| Output current | $I_{DACOUT}$ | | -10 | — | +10 | mA |
| DAC clock frequency | $f_{DAC}$ | | — | — | 1 | MHz |
| Sample rate | $SR_{DAC}$ | $f_{DAC} = f_{DAC(max)}$ | — | — | 500 | ksps |
| Resolution | $N_{RESOLUTION}$ | | — | 12 | — | bits |
| Load capacitance[1] | $C_{LOAD}$ | High-power and Low-power modes | — | — | 50 | pF |
| | | High-capacitance load mode | 25 | — | — | nF |
| Load resistance | $R_{LOAD}$ | | 5 | — | — | kΩ |
| Current consumption, Dynamic, 500 ksps, 1 channel active[2] | $I_{DAC\_1\_500}$ | High-power mode | — | 345 | — | µA |
| | | Low-power mode | — | 245 | — | µA |
| Current consumption, Dynamic, 500 ksps, 2 channels active[2] | $I_{DAC\_2\_500}$ | High-power mode | — | 531 | — | µA |
| | | Low-power mode | — | 335 | — | µA |
| Current consumption, Static, 1 channel active[3] | $I_{DAC\_1\_STAT}$ | High-power mode | — | 134 | — | µA |
| | | Low-power mode | — | 30 | — | µA |
| | | High-capacitance mode | — | 42 | — | µA |
| Current consumption, Static, 2 channels active[3] | $I_{DAC\_2\_STAT}$ | High-power mode | — | 261 | 400 | µA |
| | | Low-power mode | — | 53 | 90 | µA |
| | | High-capacitance mode | — | 77 | — | µA |
| Startup time | $t_{DACSTARTUP}$ | Enable to 90% full scale output, settling to 10 LSB | — | 4.2 | 4.7 | µs |
| Settling time | $t_{DACSETTLE}$ | High-power mode, 25% to 75% of full scale, settling to 10 LSB | — | 1.1 | 1.6 | µs |
| | | Low-power mode, 25% to 75% of full scale, settling to 1% | — | 2.7 | — | µs |
| Output impedance | $R_{OUT}$ | Main output, High-power mode | — | 2.4 | — | Ω |
| | | Main output, Low-power mode | — | 3.3 | — | Ω |
| Power supply rejection ratio[4] | PSRR | Vout = 50% full scale, DC output | — | 84.4 | — | dB |
| Signal to noise and distortion ratio | $SNDR_{DAC}$ | High-power mode, 500 ksps, internal 2.5 V reference, 1 kHz sine wave input, BW limited to 250 kHz | 64.8 | 66.8 | — | dB |
| | | High-power mode, 500 ksps, internal 2.5 V reference, 1 kHz sine wave input, BW limited to 22 kHz | 68.2 | 70.7 | — | dB |
| Total Harmonic Distortion | THD | High-power mode, internal 2.5 V reference, 1 kHz sine wave input | — | -71.3 | -67.2 | dB |
| Integral Non-Linearity | $INL_{DAC}$ | High-power mode, Across full temperature range | -5 | — | 5 | LSB |
| Differential Non-Linearity[5] | $DNL_{DAC}$ | High-power mode, Across full temperature range | -1 | — | 1.3 | LSB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Offset error[6] | $V_{OFFSET}$ | High-power mode | -15 | — | 15 | mV |
| | | Low-power mode | -25 | — | 25 | mV |
| | | High-capacitance load mode | -40 | — | 40 | mV |
| Gain error[6] | $V_{GAIN}$ | 1.25 V internal reference | -1.5 | — | 1.5 | % |
| | | 2.5 V internal reference | -2 | — | 2 | % |
| | | External Reference | -0.6 | — | 0.6 | % |
| External Reference Voltage[7] | $V_{EXTREF}$ | | 1.1 | — | V_AVDD | V |

**Note:**

1. Main outputs only.
2. Dynamic current specifications are for VDAC circuitry operating at max clock frequency with the output updated at the specified sampling rate using DMA transfers. Output is a 1 kHz sine wave from 10% to 90% full scale. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
3. Static current specifications are for VDAC circuitry operating after a one-time update to a static output at 50% full scale, with the VDAC APB clock disabled. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
4. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$.
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
7. External reference voltage on PA00 when used for VREFP

### 4.15 Temperature Sensor

**Table 4.45. Temperature Sensor**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor range[1] | $T_{RANGE}$ | | -40 | — | 125 | °C |
| Temperature sensor resolution | $T_{RESOLUTION}$ | | — | 0.25 | — | °C |
| Measurement noise (RMS) | $T_{NOISE}$ | Single measurement | — | 0.6 | — | °C |
| | | 16-sample average (TEMPAVGNUM = 0) | — | 0.17 | — | °C |
| | | 64-sample average (TEMPAVGNUM = 1) | — | 0.12 | — | °C |
| Temperature offset | $T_{OFF}$ | Mean error of uncorrected output across full temperature range | — | 0.84 | — | °C |
| Temperature sensor accuracy[2] [3] | $T_{ACC}$ | Direct output accuracy after mean error ($T_{OFF}$) removed | — | +/-3 | — | °C |
| | | After linearization in software, no calibration | — | +/-2 | — | °C |
| | | After linearization in software, with single-temperature calibration at 25 °C[4] | — | +/-1.5 | — | °C |
| Measurement interval | $t_{MEAS}$ | | — | 250 | — | ms |

**Note:**

1. The sensor reports absolute die temperature in Kelvin (K). All specifications are in °C to match the units of the specified product temperature range.
2. Error is measured as the deviation of the mean temperature reading from the expected die temperature. Accuracy numbers represent statistical minimum and maximum using ± 4 standard deviations of measured error.
3. The raw output of the temperature sensor is a predictable curve. It can be linearized with a polynomial function for additional accuracy.
4. Assuming calibration accuracy of ± 0.25 °C.

## 4.16 Brown Out Detectors

### 4.16.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

**Table 4.46. DVDD BOD**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BOD threshold | $V_{DVDD\_BOD}$ | Supply rising | — | 1.68 | 1.71 | V |
| | | Supply falling | 1.62 | 1.65 | — | V |
| BOD response time | $t_{DVDD\_BOD\_DELAY}$ | Supply dropping at 100 mV / µs slew rate[1] | — | 0.95 | — | µs |
| BOD hysteresis | $V_{DVDD\_BOD\_HYST}$ | | — | 22 | — | mV |

**Note:**

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (for example, if the supply ramps down and then back up at a very fast rate).

### 4.16.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

**Table 4.47. LE DVDD BOD**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BOD threshold | $V_{DVDD\_LE\_BOD}$ | Supply falling | 1.5 | — | 1.71 | V |
| BOD response time | $t_{DVDD\_LE\_BOD\_DELAY}$ | Supply dropping at 2 mV / µs slew rate[1] | — | 55 | — | µs |
| BOD hysteresis | $V_{DVDD\_LE\_BOD\_HYST}$ | | — | 20 | — | mV |

**Note:**

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (for example, if the supply ramps down and then back up at a very fast rate).

### 4.16.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

**Table 4.48. AVDD and IOVDD BODs**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BOD threshold | $V_{BOD}$ | Supply falling | 1.45 | — | 1.71 | V |
| BOD response time | $t_{BOD\_DELAY}$ | Supply dropping at 2 mV / µs slew rate[1] | — | 55 | — | µs |
| BOD hysteresis | $V_{BOD\_HYST}$ | | — | 20 | — | mV |

**Note:**

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (for example, if the supply ramps down and then back up at a very fast rate).

### 4.17 Pulse Counter

**Table 4.49. Pulse Counter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input frequency | $F_{IN}$ | Asynchronous Single and Quadrature Modes | — | — | 1.0 | MHz |
| | | Sampled Modes with Debounce filter set to 0. | — | — | 8 | kHz |
| Setup time in asynchronous external clock mode | $t_{SU\_S1N\_S0N}$ | S1N (data) to S0N (clock) | 54 | — | — | ns |
| Hold time in asynchronous external clock mode | $t_{HD\_S0N\_S1N}$ | S0N (clock) to S1N (data) | 47 | — | — | ns |

### 4.18 EUSART SPI Main Timing

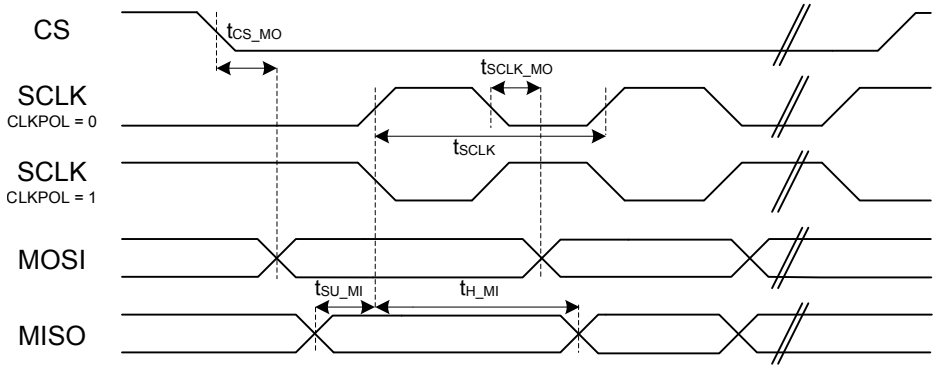



**Figure 4.1. SPI Main Timing**

### 4.18.1 EUSART SPI Main Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.50. EUSART SPI Main Timing, Voltage Scaling = VSCALE2**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period[1 2 3] | $t_{SCLK}$ | | tclk | — | — | ns |
| CS to MOSI[1 2] | $t_{CS\_MO}$ | | -11 | — | 7 | ns |
| SCLK to MOSI[1 2] | $t_{SCLK\_MO}$ | | -3 | — | 8 | ns |
| MISO setup time[1 2] | $t_{SU\_MI}$ | | 6 | — | — | ns |
| MISO hold time[1 2] | $t_{H\_MI}$ | | -21 | — | — | ns |

**Note:**

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measured using 15 pF output loading at 10% and 90% of $V_{DD}$.
3. $t_{CLK}$ is one period of the selected peripheral clock: EM01GRPCCLK for EUSART1/2, EUSART0CLK for EUSART0.

### 4.19 EUSART SPI Secondary Timing

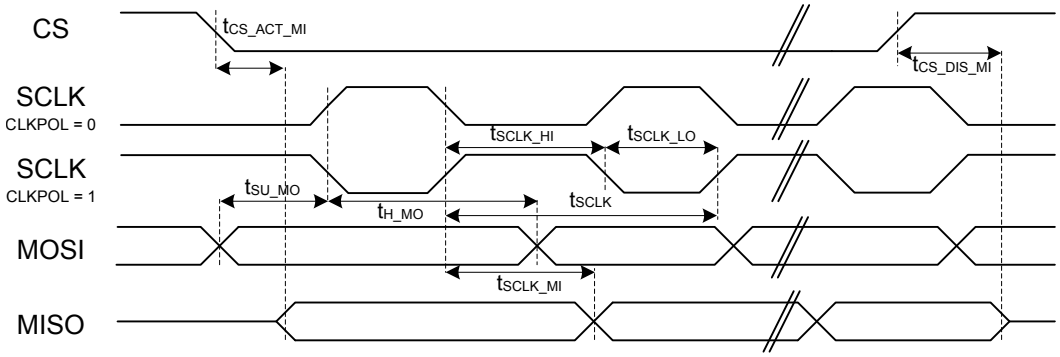



**Figure 4.2. SPI Secondary Timing**

### 4.19.1 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.51. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK high time[1] [2] | $t_{SCLK\_HI}$ | | 50 | — | — | ns |
| SCLK low time[1] [2] | $t_{SCLK\_LO}$ | | 50 | — | — | ns |
| CS active to MISO[1] [2] | $t_{CS\_ACT\_MI}$ | | 5 | — | 55 | ns |
| CS disable to MISO[1] [2] | $t_{CS\_DIS\_MI}$ | | 5 | — | 41 | ns |
| MOSI setup time[1] [2] | $t_{SU\_MO}$ | | 5 | — | — | ns |
| MOSI hold time[1] [2] | $t_{H\_MO}$ | | 7 | — | — | ns |
| SCLK to MISO[1] [2] | $t_{SCLK\_MI}$ | IOVDD = 1.8 V | 9 | — | 40 | ns |
| | | IOVDD = 3.3 V | 9 | — | 30 | ns |

**Note:**

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measured using 15 pF output loading at 10% and 90% of $V_{DD}$ (timing diagram shows 50% of $V_{DD}$).

### 4.19.2 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0

Timing specifications at VSCALE0 apply to EUSART0 only, routed to DBUSAB on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.52. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK high time[1] [2] | $t_{SCLK\_HI}$ | | 100 | — | — | ns |
| SCLK low time[1] [2] | $t_{SCLK\_LO}$ | | 100 | — | — | ns |
| CS active to MISO[1] [2] | $t_{CS\_ACT\_MI}$ | | 8 | — | 110 | ns |
| CS disable to MISO[1] [2] | $t_{CS\_DIS\_MI}$ | | 8 | — | 76 | ns |
| MOSI setup time[1] [2] | $t_{SU\_MO}$ | | 10 | — | — | ns |
| MOSI hold time[1] [2] | $t_{H\_MO}$ | | 33 | — | — | ns |
| SCLK to MISO[1] [2] | $t_{SCLK\_MI}$ | IOVDD = 1.8 V | 12 | — | 93 | ns |
| | | IOVDD = 3.3 V | 12 | — | 84 | ns |

**Note:**

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measured using 15 pF output loading at 10% and 90% of $V_{DD}$ (timing diagram shows 50% of $V_{DD}$).

## 4.20 I2C Electrical Specifications

### 4.20.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

**Table 4.53. I2C Standard-mode (Sm)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[1] | $f_{SCL}$ | | 0 | — | 100 | kHz |
| SCL clock low time | $t_{LOW}$ | | 4.7 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 4 | — | — | µs |
| SDA set-up time | $t_{SU\_DAT}$ | | 250 | — | — | ns |
| SDA hold time | $t_{HD\_DAT}$ | | 0 | — | — | ns |
| Repeated START condition set-up time | $t_{SU\_STA}$ | | 4.7 | — | — | µs |
| Repeated START condition hold time | $t_{HD\_STA}$ | | 4.0 | — | — | µs |
| STOP condition set-up time | $t_{SU\_STO}$ | | 4.0 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 4.7 | — | — | µs |

**Note:**

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. Set CLKDIV to a value that keeps the SCL clock frequency below the max value listed.

### 4.20.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

**Table 4.54. I2C Fast-mode (Fm)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[1] | $f_{SCL}$ | | 0 | — | 400 | kHz |
| SCL clock low time | $t_{LOW}$ | | 1.3 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 0.6 | — | — | µs |
| SDA set-up time | $t_{SU\_DAT}$ | | 100 | — | — | ns |
| SDA hold time | $t_{HD\_DAT}$ | | 0 | — | — | ns |
| Repeated START condition set-up time | $t_{SU\_STA}$ | | 0.6 | — | — | µs |
| Repeated START condition hold time | $t_{HD\_STA}$ | | 0.6 | — | — | µs |
| STOP condition set-up time | $t_{SU\_STO}$ | | 0.6 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 1.3 | — | — | µs |

**Note:**

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. Set CLKDIV to a value that keeps the SCL clock frequency below the max value listed.

### 4.20.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

**Table 4.55. I2C Fast-mode Plus (Fm+)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[1] | $f_{SCL}$ | | 0 | — | 1000 | kHz |
| SCL clock low time | $t_{LOW}$ | | 0.5 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 0.26 | — | — | µs |
| SDA set-up time | $t_{SU\_DAT}$ | | 50 | — | — | ns |
| SDA hold time | $t_{HD\_DAT}$ | | 0 | — | — | ns |
| Repeated START condition set-up time | $t_{SU\_STA}$ | | 0.26 | — | — | µs |
| Repeated START condition hold time | $t_{HD\_STA}$ | | 0.26 | — | — | µs |
| STOP condition set-up time | $t_{SU\_STO}$ | | 0.26 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 0.5 | — | — | µs |

**Note:**

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. Set CLKDIV to a value that keeps the SCL clock frequency below the max value listed.

### 4.21 Boot Timing

Secure boot impacts the recovery time from all sources of device reset. In addition to the root code authentication process, which cannot be disabled or bypassed, the root code can authenticate a bootloader, and the bootloader can authenticate the application. In projects that include only an application and no bootloader, the root code can authenticate the application directly. The duration of each authentication operation depends on two factors: the computation of the associated image hash, which is proportional to the size of the image, and the verification of the image signature, which is independent of image size.

The duration for the root code to authenticate the bootloader will depend on the SE firmware version as well as on the size of the bootloader.

The duration for the bootloader to authenticate the application can depend on the size of the application.

The configurations below assume that the associated bootloader and application code images do not contain a bootloader certificate or an application certificate. Authenticating a bootloader certificate or an application certificate will extend the boot time by an additional 6 to 7 ms.

The table below provides the durations from the termination of reset until the completion of the secure boot process (start of main() function in the application image) under various conditions.

Conditions:

- SE firmware version: 2.1.7
- Gecko Bootloader size: 10.1 KB

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

**Table 4.56. Boot Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Boot time | $t_{BOOT}$ | Secure boot application check disabled, no bootloader | — | 31.6 | — | ms |
| | | Secure boot application check disabled, second stage bootloader check enabled[1], 50 KB application size | — | 37.6 | — | ms |
| | | Secure boot application check enabled, second stage bootloader check enabled[1], 50 KB application size | — | 47.9 | — | ms |
| | | Secure boot application check enabled, second stage bootloader check enabled[1], 150 KB application size | — | 49.8 | — | ms |
| | | Secure boot application check enabled, second stage bootloader check enabled[1], 350 KB application size | — | 53.9 | — | ms |

**Note:**

1. Timing is measured with the specified bootloader size. Actual bootloader size impacts the boot timing slightly, with a similar µs / KB ratio as application size.

### 4.22 Crypto Operation Timing for SE Manager API

Values in this table represent timing from SE Manager API call to return. The Cortex-M33 HCLK frequency is 39.0 MHz. The timing specifications below are measured at the SE Manager function call API. Each duration in the table contains some portion that is influenced by SE Manager build compilation and Cortex-M33 operating frequency and some portion that is influenced by the Hardware Secure Engine's firmware version and its operating speed (typically 80 MHz). The contributions of the Cortex-M33 properties to the overall specification timing are most pronounced for the shorter operations such as AES and hash when operating on small payloads. The overhead of command processing at the mailbox interface can also dominate the timing for shorter operations.

Conditions:

- SE firmware version: 2.1.7
- GSDK version: 4.0.0

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

**Table 4.57. Crypto Operation Timing for SE Manager API**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AES-128 timing | $t_{AES128}$ | AES-128 CCM encryption, PT 1 KB | — | 560 | — | µs |
| | | AES-128 CCM encryption, PT 32 KB | — | 1746 | — | µs |
| | | AES-128 CTR encryption, PT 1 KB | — | 464 | — | µs |
| | | AES-128 CTR encryption, PT 32 KB | — | 1032 | — | µs |
| | | AES-128 GCM encryption, PT 1 KB | — | 512 | — | µs |
| | | AES-128 GCM encryption, PT 32 KB | — | 1073 | — | µs |
| AES-256 timing | $t_{AES256}$ | AES-256 CCM encryption, PT 1 KB | — | 573 | — | µs |
| | | AES-256 CCM encryption, PT 32 KB | — | 2181 | — | µs |
| | | AES-256 CTR encryption, PT 1 KB | — | 471 | — | µs |
| | | AES-256 CTR encryption, PT 32 KB | — | 1242 | — | µs |
| | | AES-256 GCM encryption, PT 1 KB | — | 519 | — | µs |
| | | AES-256 GCM encryption, PT 32 KB | — | 1289 | — | µs |
| ECC P-256 timing | $t_{ECC\_P256}$ | ECC key generation, P-256 | — | 5.5 | — | ms |
| | | ECC signing, P-256 | — | 5.9 | — | ms |
| | | ECC verification, P-256 | — | 6.2 | — | ms |
| ECC P-521 timing[1] | $t_{ECC\_P521}$ | ECC key generation, P-521 | — | 30.5 | — | ms |
| | | ECC signing, P-521 | — | 31.0 | — | ms |
| | | ECC verification, P-521 | — | 36.2 | — | ms |
| ECC Ed25519 timing[2] | $t_{ECCED25519}$ | ECC key generation, Ed25519 | — | 4.5 | — | ms |
| | | EdDSA signing, Ed25519 | — | 8.9 | — | ms |
| | | ECC verification, Ed25519 | — | 6.3 | — | ms |
| ECDH compute secret timing | $t_{ECDH}$ | ECDH compute secret, P-521[1] | — | 30.3 | — | ms |
| | | ECDH compute secret, Ed25519[2] | — | 4.5 | — | ms |
| | | ECDH compute secret, P-256 | — | 5.7 | — | ms |
| ECJPAKE client timing | $t_{ECJPAKE\_C}$ | ECJPAKE client write round one | — | 21.4 | — | ms |
| | | ECJPAKE client read round one | — | 11.8 | — | ms |
| | | ECJPAKE client write round two | — | 15.3 | — | ms |
| | | ECJPAKE client read round two | — | 6.4 | — | ms |
| | | ECJPAKE client derive secret | — | 8.8 | — | ms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ECJPAKE server timing | $t_{ECJPAKE\_S}$ | ECJPAKE server write round one | — | 21.5 | — | ms |
| | | ECJPAKE server read round one | — | 11.7 | — | ms |
| | | ECJPAKE server write round two | — | 15.3 | — | ms |
| | | ECJPAKE server read round two | — | 6.3 | — | ms |
| | | ECJPAKE server derive secret | — | 8.8 | — | ms |
| POLY-1305 timing[1] | $t_{POLY1305}$ | POLY-1305, PT 1 KB | — | 508 | — | µs |
| | | POLY-1305, PT 32 KB | — | 1171 | — | µs |
| SHA-256 timing | $t_{SHA256}$ | SHA-256, PT 1 KB | — | 303 | — | µs |
| | | SHA-256, PT 32 KB | — | 733 | — | µs |
| SHA-512 timing[1] | $t_{SHA512}$ | SHA-512, PT 1 KB | — | 301 | — | µs |
| | | SHA-512, PT 32 KB | — | 615 | — | µs |

**Note:**

1. Option is only available on OPNs with Secure Vault High feature set.
2. Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.

### 4.23 Crypto Operation Average Current for SE Manager API

Values in this table represent current consumed by security core during the operation, and represent additions to the current consumed by the Cortex-M33 application CPU due to the Hardware Secure Engine CPU and its associated crypto accelerators. The current measurements below represent the average value of the current for the duration of the crypto operation. Instantaneous peak currents may be higher.

Conditions:

- SE firmware version: 2.1.7
- GSDK version: 4.0.0

Current consumption is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

**Table 4.58. Crypto Operation Average Current for SE Manager API**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AES-128 current | $I_{AES128}$ | AES-128 CCM encryption, PT 1 KB | — | 1.0 | — | mA |
| | | AES-128 CCM encryption, PT 32 KB | — | 3.3 | — | mA |
| | | AES-128 CTR encryption, PT 1 KB | — | 0.8 | — | mA |
| | | AES-128 CTR encryption, PT 32 KB | — | 3.4 | — | mA |
| | | AES-128 GCM encryption, PT 1 KB | — | 0.9 | — | mA |
| | | AES-128 GCM encryption, PT 32 KB | — | 3.4 | — | mA |
| AES-256 current | $I_{AES256}$ | AES-256 CCM encryption, PT 1 KB | — | 1.0 | — | mA |
| | | AES-256 CCM encryption, PT 32 KB | — | 3.4 | — | mA |
| | | AES-256 CTR encryption, PT 1 KB | — | 0.9 | — | mA |
| | | AES-256 CTR encryption, PT 32 KB | — | 3.4 | — | mA |
| | | AES-256 GCM encryption, PT 1 KB | — | 0.9 | — | mA |
| | | AES-256 GCM encryption, PT 32 KB | — | 3.4 | — | mA |
| ECC P-256 current | $I_{ECCP256}$ | ECC key generation, P-256 | — | 1.6 | — | mA |
| | | ECC signing, P-256 | — | 1.6 | — | mA |
| | | ECC verification, P-256 | — | 1.6 | — | mA |
| ECC P-521 current[1] | $I_{ECCP521}$ | ECC key generation, P-521 | — | 1.8 | — | mA |
| | | ECC signing, P-521 | — | 1.8 | — | mA |
| | | ECC verification, P-521 | — | 1.8 | — | mA |
| ECC Ed25519 current[2] | $I_{ECCED25519}$ | ECC key generation, Ed25519 | — | 1.6 | — | mA |
| | | EdDSA signing, Ed25519 | — | 1.6 | — | mA |
| | | ECC verification, Ed25519 | — | 1.6 | — | mA |
| ECDH compute secret current | $I_{ECDH}$ | ECDH compute secret, P-521[1] | — | 1.8 | — | mA |
| | | ECDH compute secret, Ed25519[2] | — | 1.5 | — | mA |
| | | ECDH compute secret, P-256 | — | 1.6 | — | mA |
| ECJPAKE client current | $I_{ECJPAKE\_C}$ | ECJPAKE client write round one | — | 1.7 | — | mA |
| | | ECJPAKE client read round one | — | 1.7 | — | mA |
| | | ECJPAKE client write round two | — | 1.7 | — | mA |
| | | ECJPAKE client read round two | — | 1.6 | — | mA |
| | | ECJPAKE client derive secret | — | 1.7 | — | mA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ECJPAKE server current | $I_{ECJPAKE\_S}$ | ECJPAKE server write round one | — | 1.7 | — | mA |
| | | ECJPAKE server read round one | — | 1.7 | — | mA |
| | | ECJPAKE server write round two | — | 1.7 | — | mA |
| | | ECJPAKE server read round two | — | 1.6 | — | mA |
| | | ECJPAKE server derive secret | — | 1.7 | — | mA |
| POLY-1305 current[1] | $I_{POLY1305}$ | POLY-1305, PT 1 KB | — | 0.7 | — | mA |
| | | POLY-1305, PT 32 KB | — | 1.7 | — | mA |
| SHA-256 current | $I_{SHA256}$ | SHA-256, PT 1 KB | — | 0.8 | — | mA |
| | | SHA-256, PT 32 KB | — | 2.3 | — | mA |
| SHA-512 current[1] | $I_{SHA512}$ | SHA-512, PT 1 KB | — | 0.7 | — | mA |
| | | SHA-512, PT 32 KB | — | 2.0 | — | mA |

**Note:**

1. Option is only available on OPNs with Secure Vault High feature set.
2. Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.

### 4.24 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

### 4.24.1 Supply Current

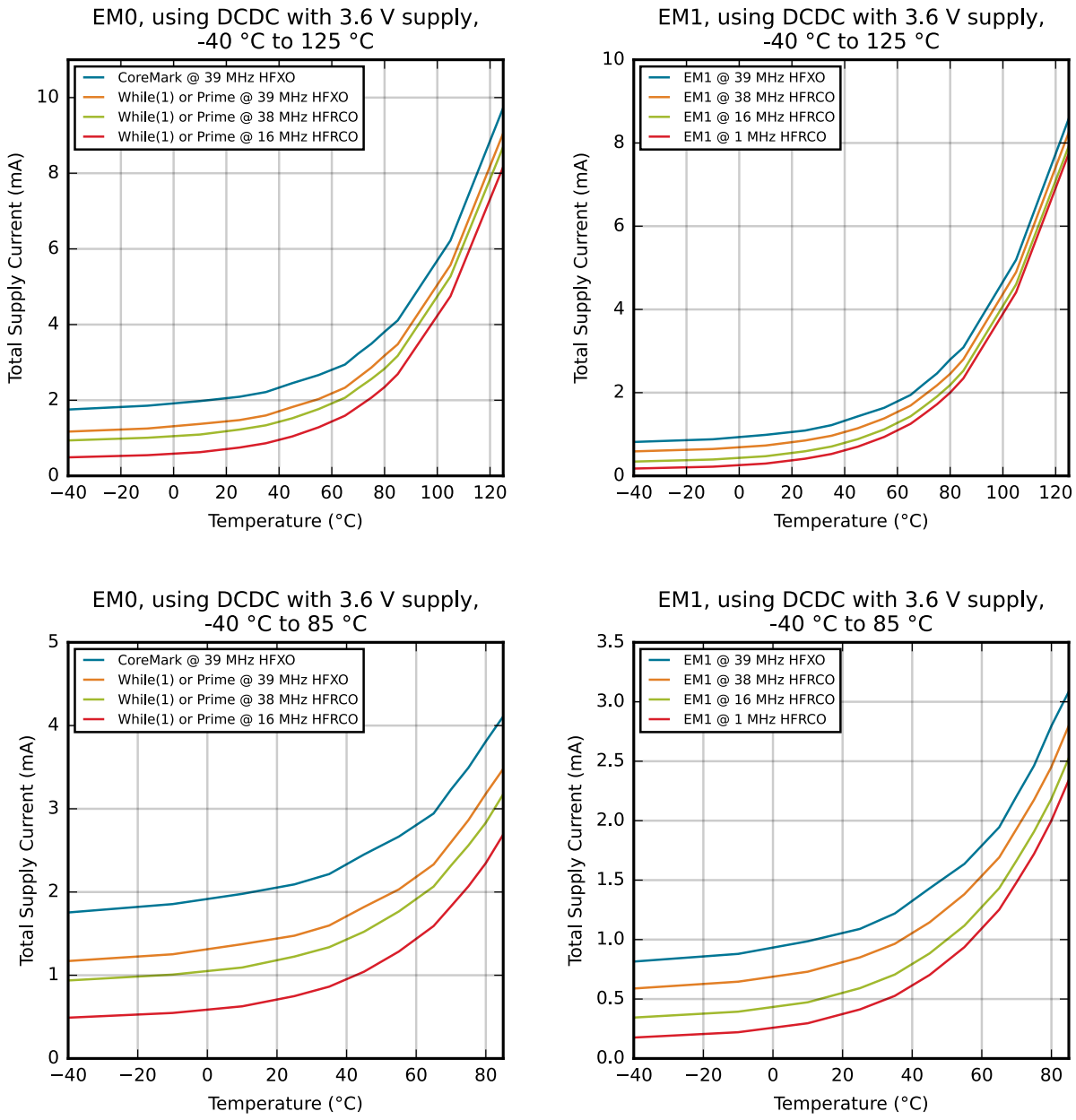



**Figure 4.3. EM0 and EM1 Typical Supply Current vs. Temperature**

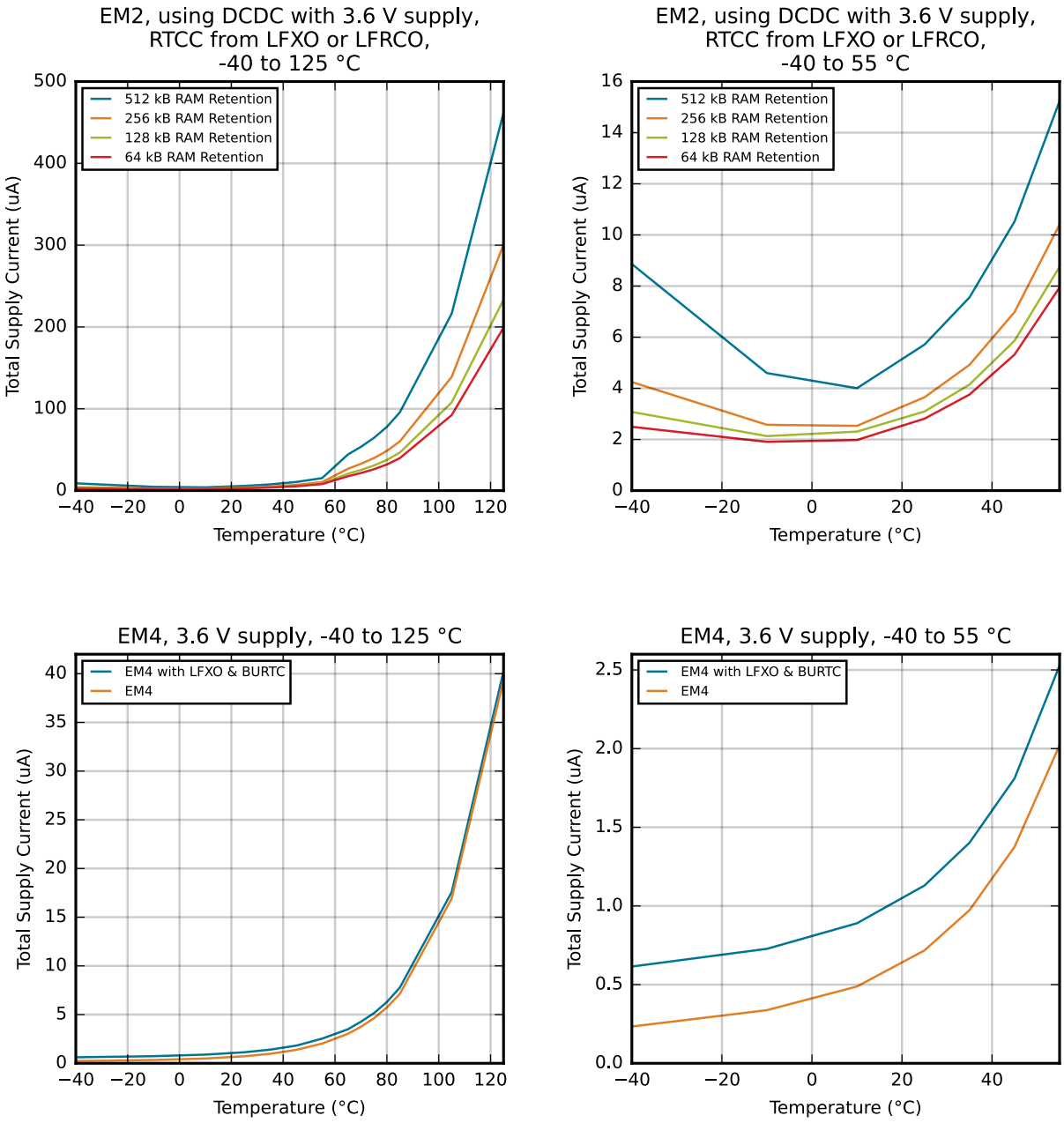



**Figure 4.4. EM2 and EM4 Typical Supply Current vs. Temperature**

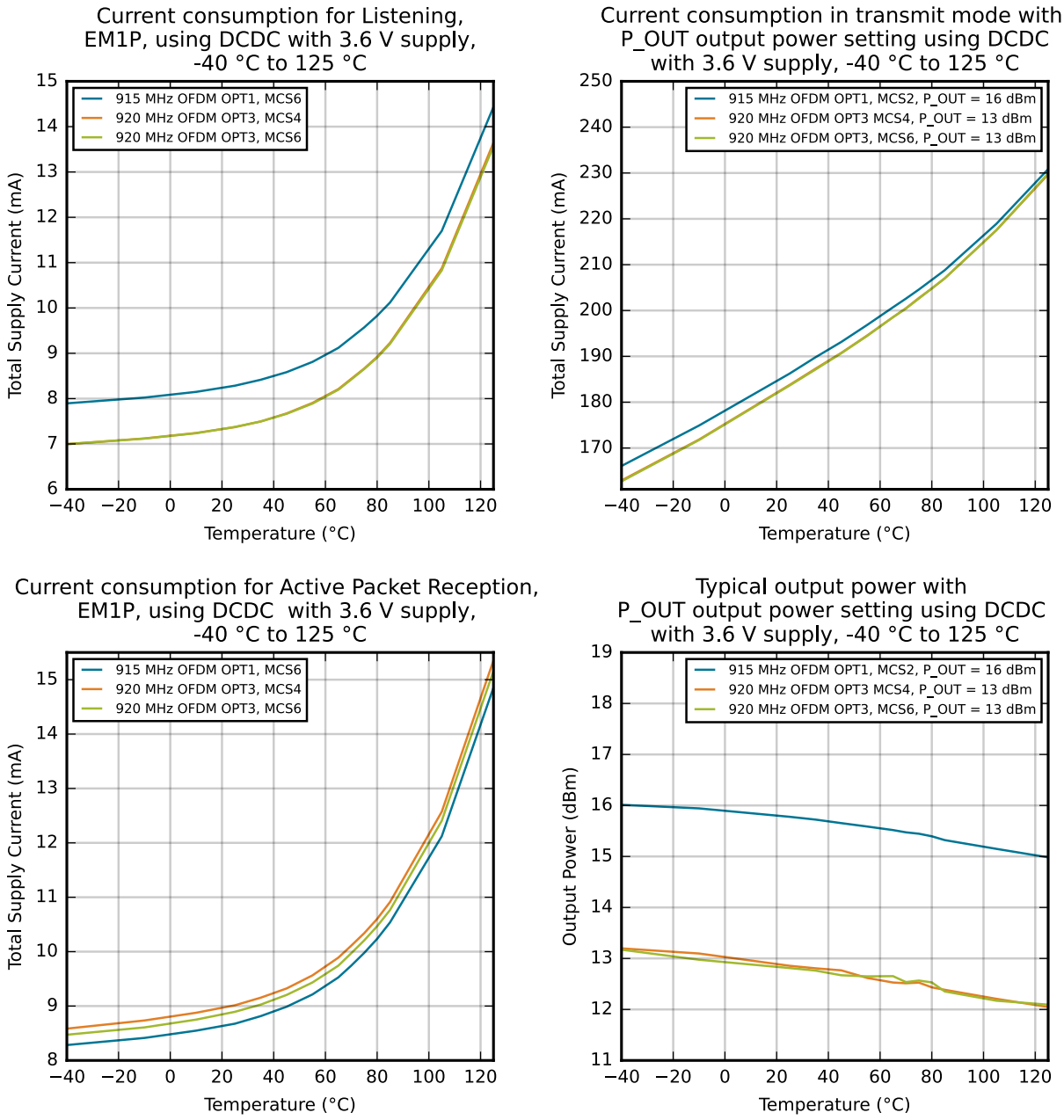



**Figure 4.5. Typical Radio Supply Current and Output Power vs. Temperature**

### 4.24.2 IADC

Typical performance is shown using 10 MHz ADC clock for fastest sampling speed and adjusting oversampling ratio (OSR).

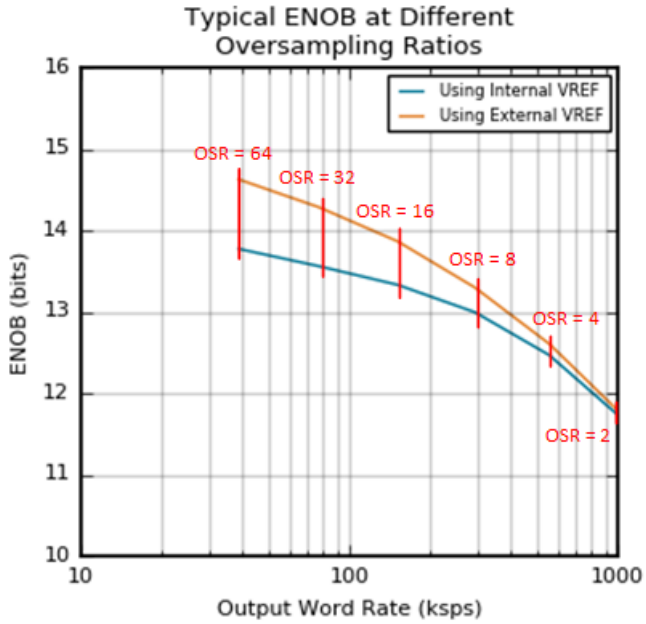



**Figure 4.6. Typical ENOB vs. Oversampling Ratio**

# 5. Typical Connection Diagrams

## 5.1 Power

Typical power supply connections are shown in the following figures.

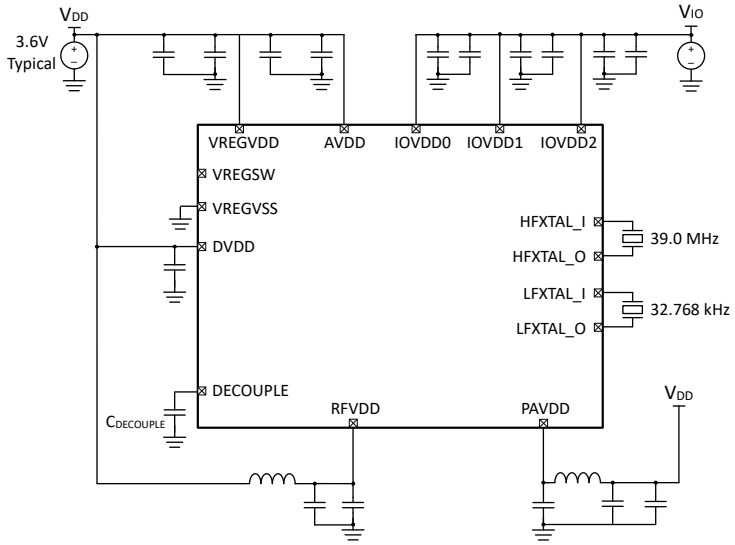



**Figure 5.1. EFR32FG25 Typical Application Circuit: Direct Supply Configuration without DCDC**

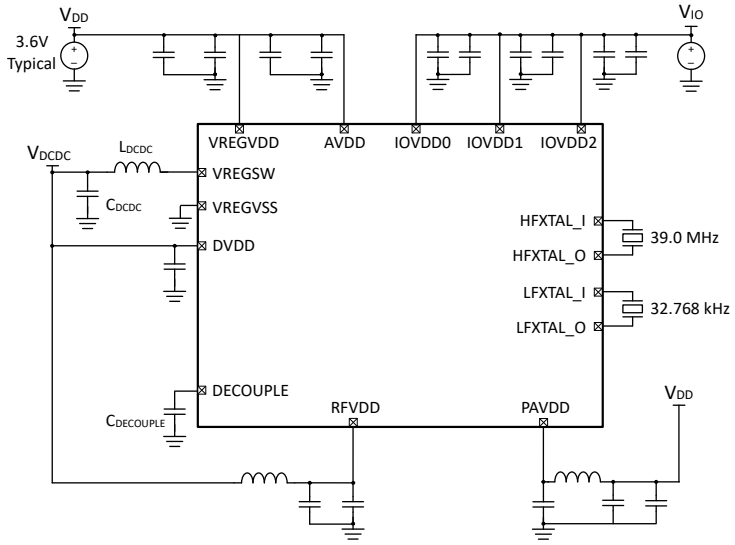



**Figure 5.2. EFR32FG25 Typical Application Circuit: DCDC Configuration**

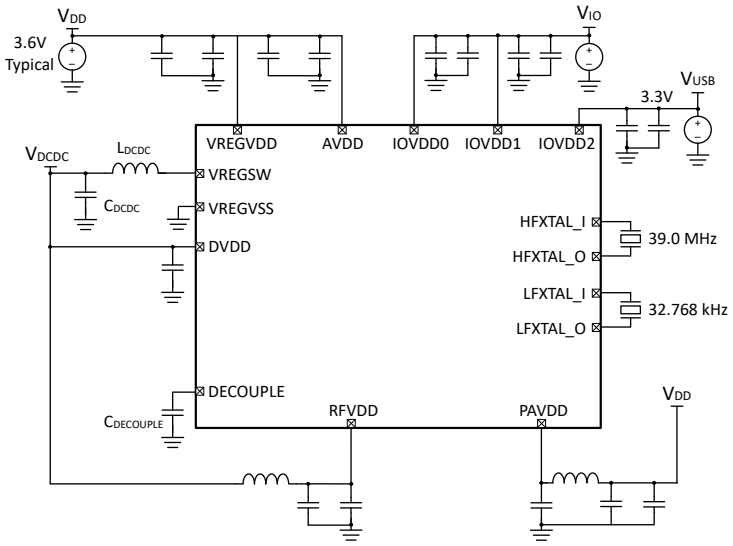



**Figure 5.3. EFR32FG25 Typical Application Circuit: DCDC Configuration, USB PHY Powered Separately**

**Note:** IOVDD2 voltage shall be supplied when the system is powered.

## 5.2 RF Matching Networks

### 5.2.1 Matching Network for 868, 915, and 920 MHz Bands

The recommended RF matching network circuit schematic for the 868, 915, and 920 MHz bands is shown in Figure 5.4. Typical Differential TX and Single Ended RX RF Impedance-matching Network Circuit for 868, 915, and 920 MHz Bands. Typical component values optimized for different RF Bands are shown in Table 5.1. RF Matching Component Values for 868, 915, and 920 MHz Bands. Please refer to the develoment board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

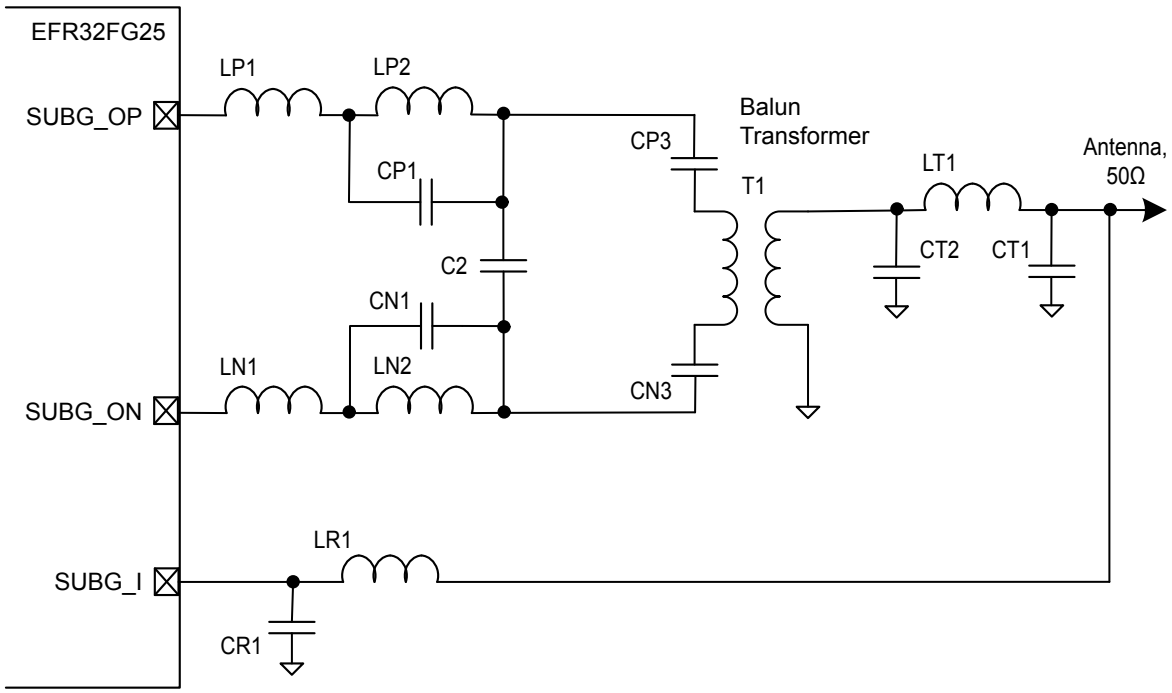



**Figure 5.4. Typical Differential TX and Single Ended RX RF Impedance-matching Network Circuit for 868, 915, and 920 MHz Bands**

**Table 5.1. RF Matching Component Values for 868, 915, and 920 MHz Bands**

| Designator | Component Value | |
|---|---|---|
| | 868 MHz | 915 & 920 MHz |
| LN1 and LP1 | 1 nH | 0.8 nH |
| LN2 and LP2 | 1 nH | 0.9 nH |
| CN1 and CP1 | 5.9 pF | 5.7 pF |
| C2 | 5.4 pF | 4.2 pF |
| CN3 and CP3 | 220 pF | 220 pF |
| T1 | MMCZ1601G7T_0088A1 | MMCZ1601G7T_0088A1 |
| LT1 | 7.5 nH | 7.5 nH |
| CT1 | 4.0 pF | 4.4 pF |
| CT2 | 2.6 pF | 2.2 pF |

| Designator | Component Value | |
|---|---|---|
| | 868 MHz | 915 & 920 MHz |
| LR1 | 18 nH | 18 nH |
| CR1 | DNP | DNP |

### 5.2.2 Matching Network for 470 MHz Band

The recommended RF matching network circuit schematic for the 470 MHz band is shown in Figure 5.5. Typical Differential TX and Single Ended RX RF Impedance-matching Network Circuit for 470 MHz Band. Typical component values optimized for different RF Bands are shown in Table 5.2. RF Matching Component Values for 470 MHz Band. Please refer to the develoment board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

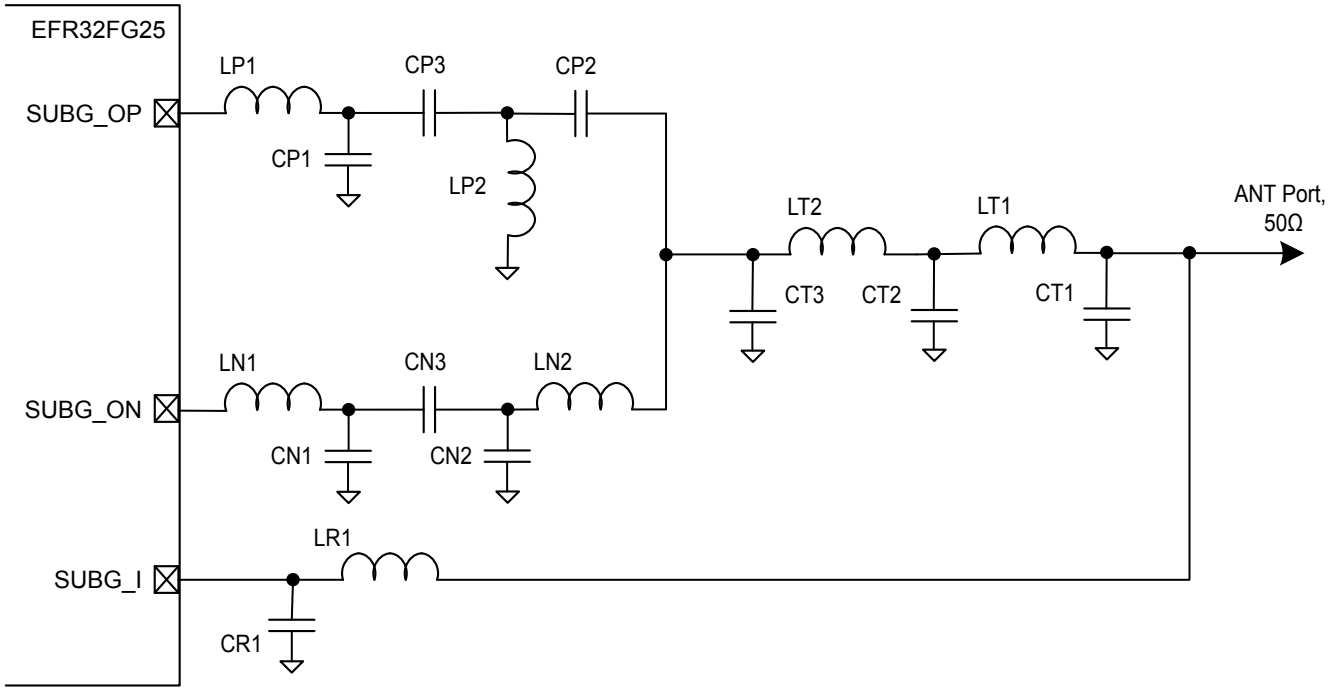



**Figure 5.5. Typical Differential TX and Single Ended RX RF Impedance-matching Network Circuit for 470 MHz Band**

**Table 5.2. RF Matching Component Values for 470 MHz Band**

| Designator | Component Value |
|---|---|
| | 470 MHz |
| LN1 and LP1 | 4.2 nH |
| LN2 and LP2 | 16 nH |
| CN1 | 18 pF |
| CP1 | 20 pF |
| CN2 | 9 pF |
| CP2 | 7 pF |
| CN3 and CP3 | 220 pF |
| LT1 | 16 nH |
| LT2 | 13 nH |
| CT1 | 5.0 pF |
| CT2 | 9.5 pF |
| CT3 | 8.0 pF |
| LR1 | 68 nH |
| CR1 | DNP |

### 5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

# 6. Pin Definitions

## 6.1 QFN56 / Standard Device Pinout

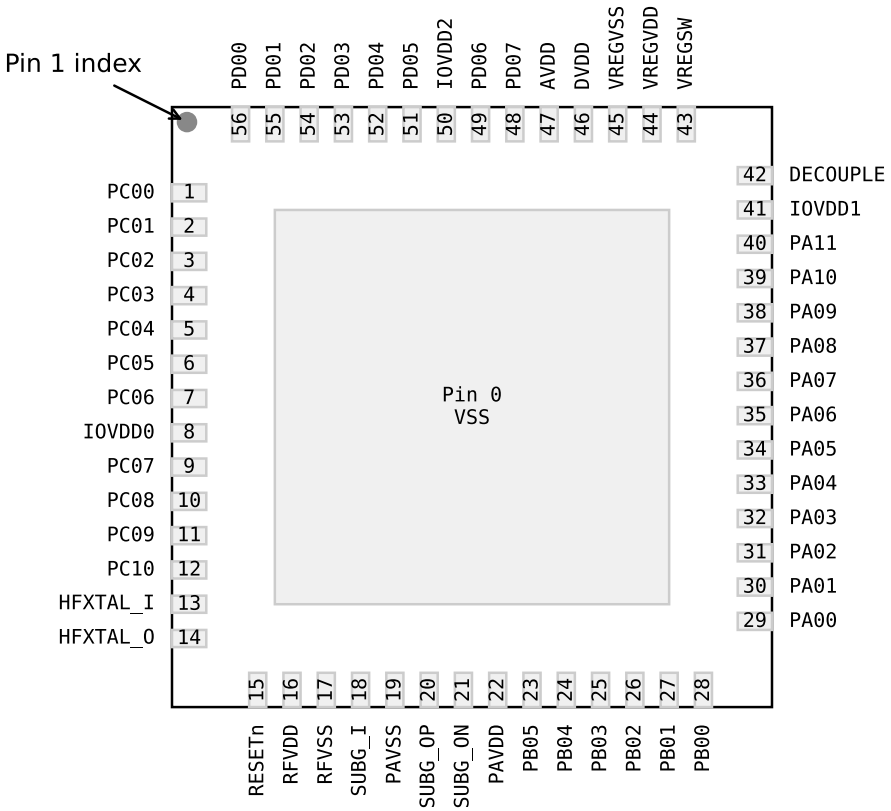



**Figure 6.1. QFN56 / Standard Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.3 Alternate Function Table, 6.4 Analog Peripheral Connectivity, and 6.5 Digital Peripheral Connectivity.

**Table 6.1. QFN56 / Standard Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PC00 | 1 | GPIO | PC01 | 2 | GPIO |
| PC02 | 3 | GPIO | PC03 | 4 | GPIO |
| PC04 | 5 | GPIO | PC05 | 6 | GPIO |
| PC06 | 7 | GPIO | IOVDD0 | 8 | IOVDD Supply 0 |
| PC07 | 9 | GPIO | PC08 | 10 | GPIO |
| PC09 | 11 | GPIO | PC10 | 12 | GPIO |
| HFXTAL_I | 13 | High-Frequency Crystal Input | HFXTAL_O | 14 | High-Frequency Crystal Output |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| RESETn | 15 | RESET | RFVDD | 16 | RFVDD Supply |
| RFVSS | 17 | RF Ground | SUBG_I | 18 | Sub-GHz Input |
| PAVSS | 19 | PA Ground | SUBG_OP | 20 | Sub-GHz Output (Positive) |
| SUBG_ON | 21 | Sub-GHz Output (Negative) | PAVDD | 22 | PAVDD Supply |
| PB05 | 23 | GPIO | PB04 | 24 | GPIO |
| PB03 | 25 | GPIO | PB02 | 26 | GPIO |
| PB01 | 27 | GPIO | PB00 | 28 | GPIO |
| PA00 | 29 | GPIO | PA01 | 30 | GPIO |
| PA02 | 31 | GPIO | PA03 | 32 | GPIO |
| PA04 | 33 | GPIO | PA05 | 34 | GPIO |
| PA06 | 35 | GPIO | PA07 | 36 | GPIO |
| PA08 | 37 | GPIO | PA09 | 38 | GPIO |
| PA10 | 39 | GPIO | PA11 | 40 | GPIO |
| IOVDD1 | 41 | IOVDD Supply 1 | DECOUPLE | 42 | Decouple Capactor |
| VREGSW | 43 | VREG Switch output | VREGVDD | 44 | VREG Input |
| VREGVSS | 45 | DCDC Ground | DVDD | 46 | Digital DVDD Supply |
| AVDD | 47 | Analog AVDD Supply | PD07 | 48 | GPIO |
| PD06 | 49 | GPIO | IOVDD2 | 50 | IOVDD Supply 2 |
| PD05 | 51 | GPIO | PD04 | 52 | GPIO |
| PD03 | 53 | GPIO | PD02 | 54 | GPIO |
| PD01 | 55 | GPIO | PD00 | 56 | GPIO |

### 6.2 QFN56 / Clock Out Device Pinout

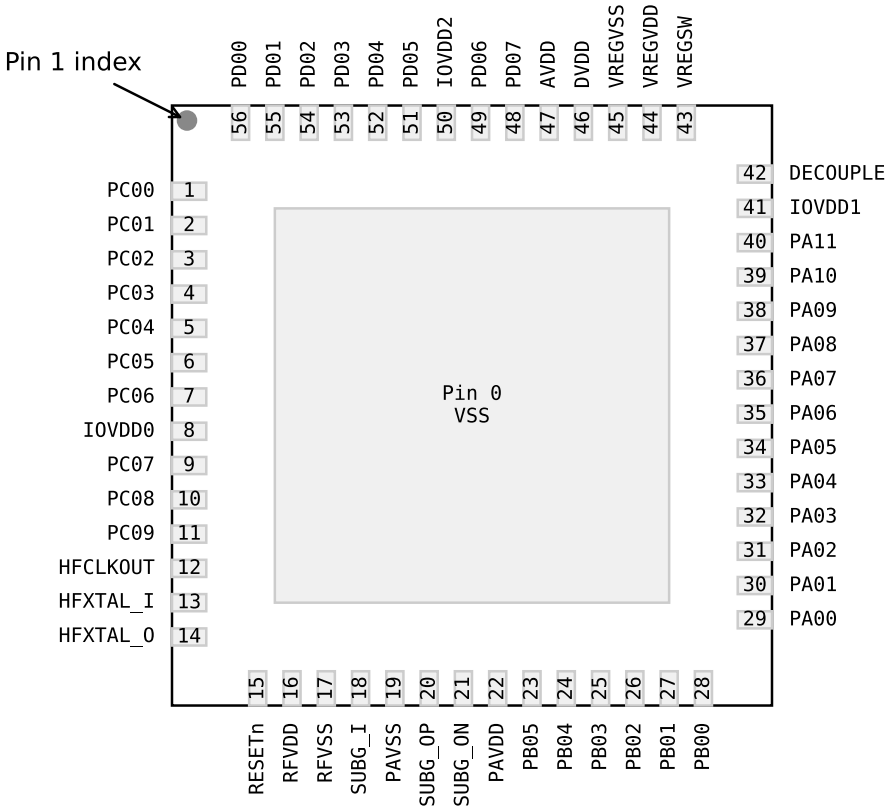



**Figure 6.2. QFN56 / Clock Out Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.3 Alternate Function Table, 6.4 Analog Peripheral Connectivity, and 6.5 Digital Peripheral Connectivity.

**Table 6.2. QFN56 / Clock Out Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PC00 | 1 | GPIO | PC01 | 2 | GPIO |
| PC02 | 3 | GPIO | PC03 | 4 | GPIO |
| PC04 | 5 | GPIO | PC05 | 6 | GPIO |
| PC06 | 7 | GPIO | IOVDD0 | 8 | IOVDD Supply 0 |
| PC07 | 9 | GPIO | PC08 | 10 | GPIO |
| PC09 | 11 | GPIO | HFCLKOUT | 12 | High-Frequency Clock Out |
| HFXTAL_I | 13 | High-Frequency Crystal Input | HFXTAL_O | 14 | High-Frequency Crystal Output |
| RESETn | 15 | RESET | RFVDD | 16 | RFVDD Supply |
| RFVSS | 17 | RF Ground | SUBG_I | 18 | Sub-GHz Input |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PAVSS | 19 | PA Ground | SUBG_OP | 20 | Sub-GHz Output (Positive) |
| SUBG_ON | 21 | Sub-GHz Output (Negative) | PAVDD | 22 | PAVDD Supply |
| PB05 | 23 | GPIO | PB04 | 24 | GPIO |
| PB03 | 25 | GPIO | PB02 | 26 | GPIO |
| PB01 | 27 | GPIO | PB00 | 28 | GPIO |
| PA00 | 29 | GPIO | PA01 | 30 | GPIO |
| PA02 | 31 | GPIO | PA03 | 32 | GPIO |
| PA04 | 33 | GPIO | PA05 | 34 | GPIO |
| PA06 | 35 | GPIO | PA07 | 36 | GPIO |
| PA08 | 37 | GPIO | PA09 | 38 | GPIO |
| PA10 | 39 | GPIO | PA11 | 40 | GPIO |
| IOVDD1 | 41 | IOVDD Supply 1 | DECOUPLE | 42 | Decouple Capactor |
| VREGSW | 43 | VREG Switch output | VREGVDD | 44 | VREG Input |
| VREGVSS | 45 | DCDC Ground | DVDD | 46 | Digital DVDD Supply |
| AVDD | 47 | Analog AVDD Supply | PD07 | 48 | GPIO |
| PD06 | 49 | GPIO | IOVDD2 | 50 | IOVDD Supply 2 |
| PD05 | 51 | GPIO | PD04 | 52 | GPIO |
| PD03 | 53 | GPIO | PD02 | 54 | GPIO |
| PD01 | 55 | GPIO | PD00 | 56 | GPIO |

### 6.3 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows GPIO pins with support for dedicated functions across the different package options.

**Table 6.3. GPIO Alternate Function Table**

| GPIO | Alternate Functions | QFN56 / Standard Package[1] | QFN56 / Clock Out Package[2] |
|---|---|---|---|
| PA01 | GPIO.SWCLK | Yes | Yes |
| PA02 | GPIO.SWDIO | Yes | Yes |
| PA03 | GPIO.SWV | Yes | Yes |
| | GPIO.TDO | Yes | Yes |
| | GPIO.TRACEDATA0 | Yes | Yes |
| | LESENSE.EN_0 | Yes | Yes |
| PA04 | GPIO.TDI | Yes | Yes |
| | GPIO.TRACECLK | Yes | Yes |
| | LESENSE.EN_1 | Yes | Yes |
| PA05 | ETAMPDET.ETAMPIN0 | Yes | Yes |
| | GPIO.TRACEDATA1 | Yes | Yes |
| | GPIO.EM4WU0 | Yes | Yes |
| | LESENSE.EN_2 | Yes | Yes |
| PA06 | ETAMPDET.ETAMPOUT0 | Yes | Yes |
| | GPIO.TRACEDATA2 | Yes | Yes |
| PA07 | GPIO.TRACEDATA3 | Yes | Yes |
| PA11 | GPIO.EM4WU1 | Yes | Yes |
| PB00 | VDAC0.CH0_MAIN_OUT | Yes | Yes |
| PB01 | GPIO.EM4WU3 | Yes | Yes |
| | VDAC0.CH1_MAIN_OUT | Yes | Yes |
| PB03 | GPIO.EM4WU4 | Yes | Yes |
| PC00 | GPIO.EM4WU6 | Yes | Yes |
| PC04 | RAC.FEM_DATA0 | Yes | Yes |
| PC05 | GPIO.EM4WU7 | Yes | Yes |
| | RAC.FEM_DATA1 | Yes | Yes |
| PC06 | RAC.FEM_DATA2 | Yes | Yes |
| PC07 | GPIO.EM4WU8 | Yes | Yes |
| | RAC.AUXADC_IN6_SHIM_EN | Yes | Yes |
| | RAC.FEM_DATA3 | Yes | Yes |
| PC08 | RAC.AUXADC_IN8_SHIM_EN | Yes | Yes |
| PC09 | GPIO.THMSW_EN | | Yes |
| | GPIO.THMSW_HALFSWITCH | | Yes |
| PC10 | GPIO.THMSW_EN | Yes | |
| | GPIO.THMSW_HALFSWITCH | Yes | |
| PD00 | LFXO.LFXTAL_O | Yes | Yes |

| GPIO | Alternate Functions | QFN56 / Standard Package[1] | QFN56 / Clock Out Package[2] |
|---|---|---|---|
| PD01 | LFXO.LFXTAL_I | Yes | Yes |
| | LFXO.LF_EXTCLK | Yes | Yes |
| PD02 | GPIO.EM4WU9 | Yes | Yes |
| PD04 | ETAMPDET.ETAMPOUT1 | Yes | Yes |
| PD05 | ETAMPDET.ETAMPIN1 | Yes | Yes |
| | GPIO.EM4WU10 | Yes | Yes |
| PD06 | USB.USB_DPLUS | Yes | Yes |
| PD07 | USB.USB_DMINUS | Yes | Yes |

**Note:**

1. QFN56 / Standard Package includes OPNs EFR32FG25A021F512IM56-B, EFR32FG25A111F1152IM56-B, EFR32FG25A121F1152IM56-B, EFR32FG25A211F1920IM56-B, EFR32FG25A221F1920IM56-B, EFR32FG25B111F1152IM56-B, EFR32FG25B121F1152IM56-B, EFR32FG25B211F1920IM56-B, and EFR32FG25B221F1920IM56-B
2. QFN56 / Clock Out Package includes OPNs EFR32FG25B212F1920IM56-B and EFR32FG25B222F1920IM56-B

### 6.4 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIOs. The following table indicates which peripherals are available on each GPIO port. When a differential connection is being used, positive inputs are restricted to the EVEN pins and negative inputs are restricted to the ODD pins. When a single-ended connection is being used, positive input is available on all pins. See the device reference manual for more details on the ABUS and analog peripherals. Note that some functions may not be available on all device variants.

**Table 6.4. ABUS Routing Table**

| Peripheral | Signal | PA | | PB | | PC | | PD | |
|---|---|---|---|---|---|---|---|---|---|
| | | EVEN | ODD | EVEN | ODD | EVEN | ODD | EVEN | ODD |
| ACMP0 | ANA_NEG | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ANA_POS | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| ACMP1 | ANA_NEG | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ANA_POS | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| IADC0 | ANA_NEG | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ANA_POS | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| VDAC0 | CH0_ABUS_OUT | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | CH1_ABUS_OUT | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

### 6.5 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIOs. The following table indicates which peripherals are available on each GPIO port. Note that some functions may not be available on all device variants.

**Table 6.5. DBUS Routing Table**

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| ACMP0.DIGOUT | Available | Available | Available | Available |
| ACMP1.DIGOUT | Available | Available | Available | Available |
| CMU.CLKIN0 | | | Available | Available |
| CMU.CLKOUT0 | | | Available | Available |
| CMU.CLKOUT1 | | | Available | Available |
| CMU.CLKOUT2 | Available | Available | | |
| EUSART0.CS | Available | Available | | |
| EUSART0.CTS | Available | Available | | |
| EUSART0.RTS | Available | Available | | |
| EUSART0.RX | Available | Available | | |
| EUSART0.SCLK | Available | Available | | |
| EUSART0.TX | Available | Available | | |
| EUSART1.CS | Available | Available | Available | Available |
| EUSART1.CTS | Available | Available | Available | Available |
| EUSART1.RTS | Available | Available | Available | Available |
| EUSART1.RX | Available | Available | Available | Available |
| EUSART1.SCLK | Available | Available | Available | Available |
| EUSART1.TX | Available | Available | Available | Available |
| EUSART2.CS | | | Available | Available |
| EUSART2.CTS | | | Available | Available |
| EUSART2.RTS | | | Available | Available |
| EUSART2.RX | | | Available | Available |
| EUSART2.SCLK | | | Available | Available |
| EUSART2.TX | | | Available | Available |
| EUSART3.CS | Available | Available | | |
| EUSART3.CTS | Available | Available | | |
| EUSART3.RTS | Available | Available | | |
| EUSART3.RX | Available | Available | | |
| EUSART3.SCLK | Available | Available | | |
| EUSART3.TX | Available | Available | | |
| EUSART4.CS | | | Available | Available |
| EUSART4.CTS | | | Available | Available |
| EUSART4.RTS | | | Available | Available |
| EUSART4.RX | | | Available | Available |
| EUSART4.SCLK | | | Available | Available |

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| EUSART4.TX | | | Available | Available |
| FRC.DCLK | | | Available | Available |
| FRC.DFRAME | | | Available | Available |
| FRC.DOUT | | | Available | Available |
| HFXO0.BUFOUT_REQ_IN_ASYNC | Available | Available | | |
| I2C0.SCL | Available | Available | Available | Available |
| I2C0.SDA | Available | Available | Available | Available |
| I2C1.SCL | | | Available | Available |
| I2C1.SDA | | | Available | Available |
| LESENSE.CH0OUT | Available | Available | | |
| LESENSE.CH1OUT | Available | Available | | |
| LESENSE.CH2OUT | Available | Available | | |
| LESENSE.CH3OUT | Available | Available | | |
| LESENSE.CH4OUT | Available | Available | | |
| LESENSE.CH5OUT | Available | Available | | |
| LESENSE.CH6OUT | Available | Available | | |
| LESENSE.CH7OUT | Available | Available | | |
| LESENSE.CH8OUT | Available | Available | | |
| LESENSE.CH9OUT | Available | Available | | |
| LESENSE.CH10OUT | Available | Available | | |
| LESENSE.CH11OUT | Available | Available | | |
| LESENSE.CH12OUT | Available | Available | | |
| LESENSE.CH13OUT | Available | Available | | |
| LESENSE.CH14OUT | Available | Available | | |
| LESENSE.CH15OUT | Available | Available | | |
| LETIMER0.OUT0 | Available | Available | | |
| LETIMER0.OUT1 | Available | Available | | |
| MODEM.ANT0 | Available | Available | Available | Available |
| MODEM.ANT1 | Available | Available | Available | Available |
| MODEM.ANT_ROLL_OVER | | | Available | Available |
| MODEM.ANT_RR0 | | | Available | Available |
| MODEM.ANT_RR1 | | | Available | Available |
| MODEM.ANT_RR2 | | | Available | Available |
| MODEM.ANT_RR3 | | | Available | Available |
| MODEM.ANT_RR4 | | | Available | Available |
| MODEM.ANT_RR5 | | | Available | Available |
| MODEM.ANT_SW_EN | | | Available | Available |
| MODEM.ANT_SW_US | | | Available | Available |
| MODEM.ANT_TRIG | | | Available | Available |
| MODEM.ANT_TRIG_STOP | | | Available | Available |

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| MODEM.DCLK | Available | Available | | |
| MODEM.DIN | Available | Available | | |
| MODEM.DOUT | Available | Available | | |
| PCNT0.S0IN | Available | Available | | |
| PCNT0.S1IN | Available | Available | | |
| PRS.ASYNCH0 | Available | Available | | |
| PRS.ASYNCH1 | Available | Available | | |
| PRS.ASYNCH2 | Available | Available | | |
| PRS.ASYNCH3 | Available | Available | | |
| PRS.ASYNCH4 | Available | Available | | |
| PRS.ASYNCH5 | Available | Available | | |
| PRS.ASYNCH6 | | | Available | Available |
| PRS.ASYNCH7 | | | Available | Available |
| PRS.ASYNCH8 | | | Available | Available |
| PRS.ASYNCH9 | | | Available | Available |
| PRS.ASYNCH10 | | | Available | Available |
| PRS.ASYNCH11 | | | Available | Available |
| PRS.SYNCH0 | Available | Available | Available | Available |
| PRS.SYNCH1 | Available | Available | Available | Available |
| PRS.SYNCH2 | Available | Available | Available | Available |
| PRS.SYNCH3 | Available | Available | Available | Available |
| TIMER0.CC0 | Available | Available | Available | Available |
| TIMER0.CC1 | Available | Available | Available | Available |
| TIMER0.CC2 | Available | Available | Available | Available |
| TIMER0.CDTI0 | Available | Available | Available | Available |
| TIMER0.CDTI1 | Available | Available | Available | Available |
| TIMER0.CDTI2 | Available | Available | Available | Available |
| TIMER1.CC0 | Available | Available | Available | Available |
| TIMER1.CC1 | Available | Available | Available | Available |
| TIMER1.CC2 | Available | Available | Available | Available |
| TIMER1.CDTI0 | Available | Available | Available | Available |
| TIMER1.CDTI1 | Available | Available | Available | Available |
| TIMER1.CDTI2 | Available | Available | Available | Available |
| TIMER2.CC0 | Available | Available | | |
| TIMER2.CC1 | Available | Available | | |
| TIMER2.CC2 | Available | Available | | |
| TIMER2.CDTI0 | Available | Available | | |
| TIMER2.CDTI1 | Available | Available | | |
| TIMER2.CDTI2 | Available | Available | | |
| TIMER3.CC0 | | | Available | Available |

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| TIMER3.CC1 | | | Available | Available |
| TIMER3.CC2 | | | Available | Available |
| TIMER3.CDTI0 | | | Available | Available |
| TIMER3.CDTI1 | | | Available | Available |
| TIMER3.CDTI2 | | | Available | Available |
| TIMER4.CC0 | Available | Available | | |
| TIMER4.CC1 | Available | Available | | |
| TIMER4.CC2 | Available | Available | | |
| TIMER4.CDTI0 | Available | Available | | |
| TIMER4.CDTI1 | Available | Available | | |
| TIMER4.CDTI2 | Available | Available | | |
| TIMER5.CC0 | | | Available | Available |
| TIMER5.CC1 | | | Available | Available |
| TIMER5.CC2 | | | Available | Available |
| TIMER5.CDTI0 | | | Available | Available |
| TIMER5.CDTI1 | | | Available | Available |
| TIMER5.CDTI2 | | | Available | Available |
| TIMER6.CC0 | Available | Available | | |
| TIMER6.CC1 | Available | Available | | |
| TIMER6.CC2 | Available | Available | | |
| TIMER6.CDTI0 | Available | Available | | |
| TIMER6.CDTI1 | Available | Available | | |
| TIMER6.CDTI2 | Available | Available | | |
| TIMER7.CC0 | | | Available | Available |
| TIMER7.CC1 | | | Available | Available |
| TIMER7.CC2 | | | Available | Available |
| TIMER7.CDTI0 | | | Available | Available |
| TIMER7.CDTI1 | | | Available | Available |
| TIMER7.CDTI2 | | | Available | Available |
| USB.USB_VBUS_SENSE | Available | Available | Available | Available |

# 7. QFN56 Package Specifications

## 7.1 QFN56 Package Dimensions

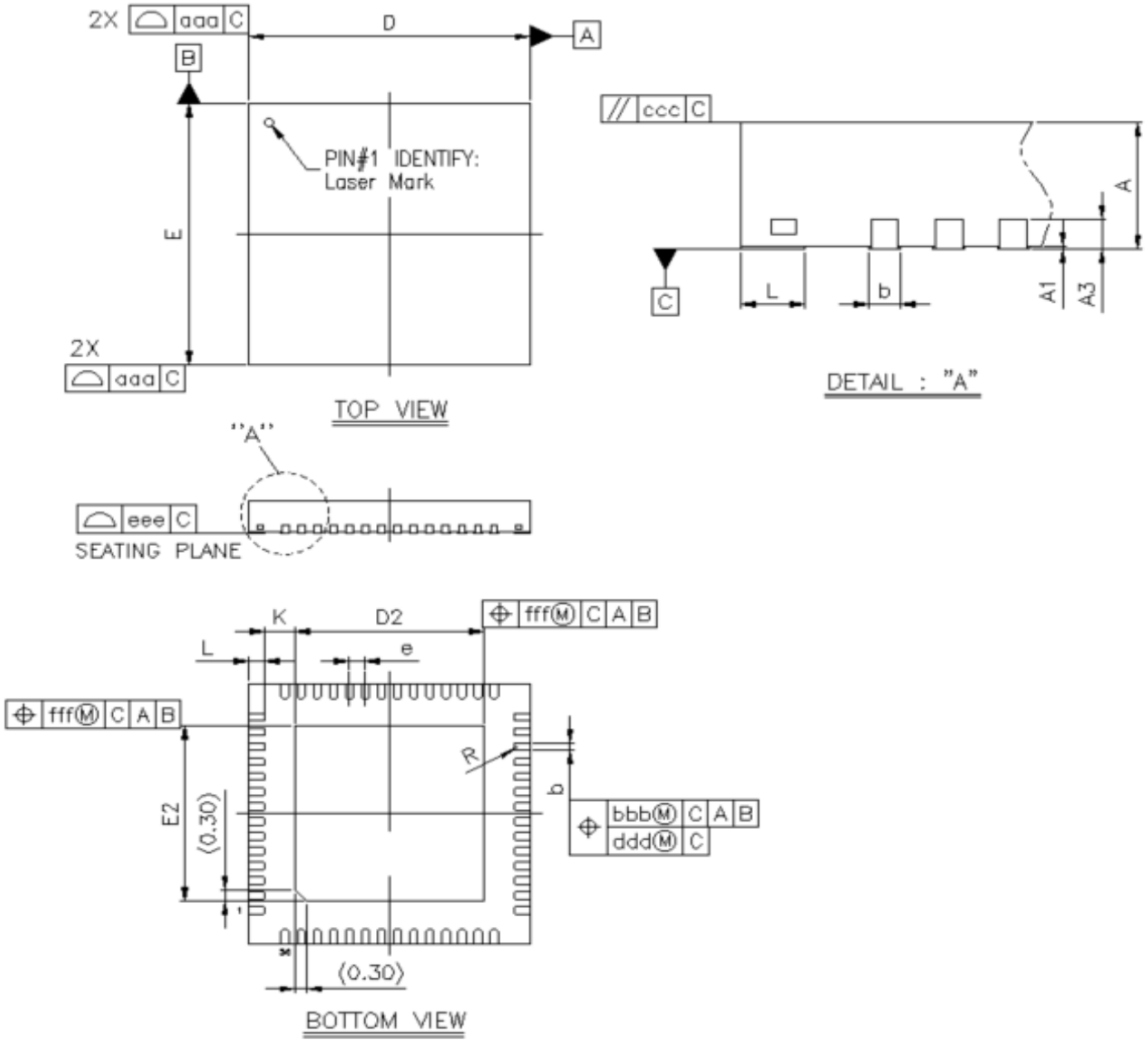



**Figure 7.1. QFN56 Package Drawing**

**Table 7.1. QFN56 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.15 | 0.20 | 0.25 |

| Dimension | Min | Typ | Max |
|---|---|---|---|
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| D2 | 4.60 | 4.70 | 4.80 |
| E2 | 4.60 | 4.70 | 4.80 |
| e | | 0.40 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| R | 0.075 | — | 0.125 |
| aaa | | 0.10 | |
| bbb | | 0.07 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-247.
4. Recommended card reflow profile is per the JEDEC J-STD-020C specification for small body, lead-free components.

### 7.2 QFN56 PCB Land Pattern

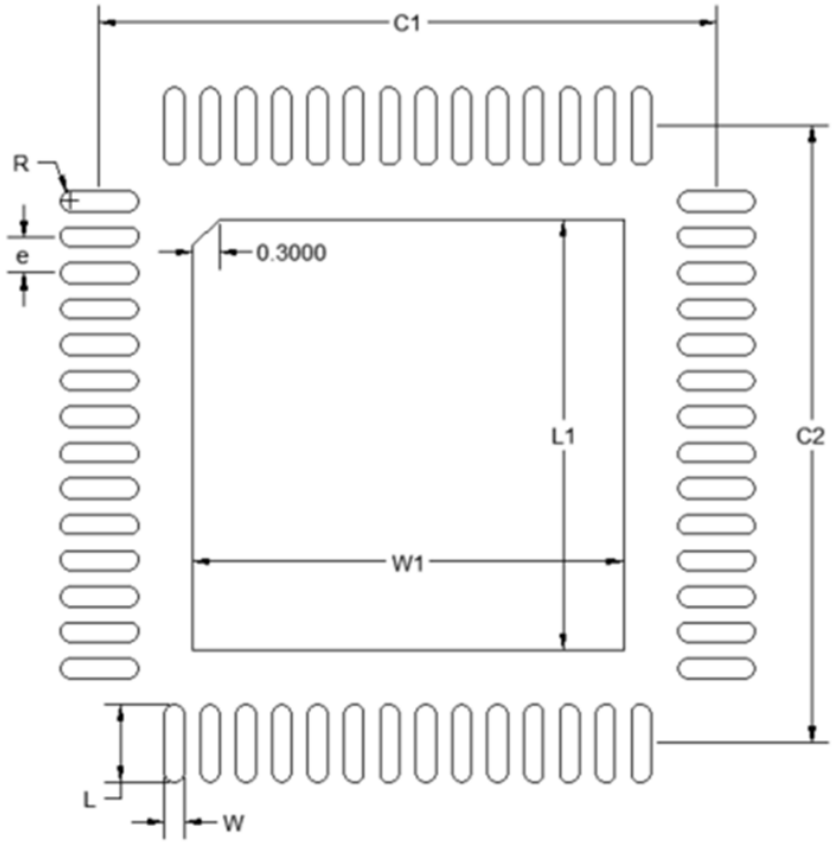



**Figure 7.2. QFN56 PCB Land Pattern Drawing**

**Table 7.2. QFN56 PCB Land Pattern Dimensions**

| Dimension | Typ |
|---|---|
| C1 | 6.87 |
| C2 | 6.87 |
| W1 | 4.80 |
| L1 | 4.80 |
| e | 0.40 |
| L | 0.86 |
| W | 0.22 |
| R | 0.11 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
5. All pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.100 mm (4 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.
11. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

### 7.3 QFN56 Package Marking

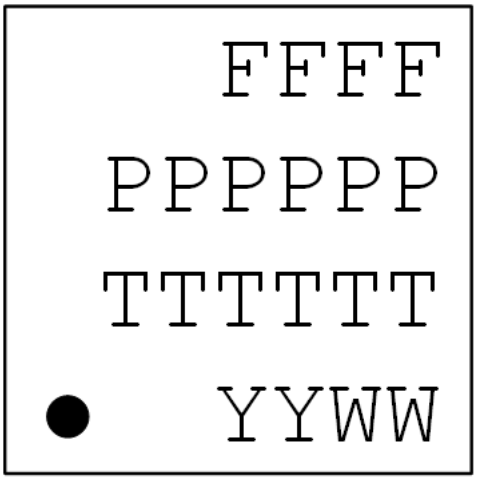



**Figure 7.3. QFN56 Package Marking**

The package marking consists of:

- FFFF – The product family codes.
  1. Family Code (F)
  2. G (Gecko)
  3. Series (2)
  4. Device Configuration (5)
- PPPPPP – The product option codes.
  - 1. Security ( A = Secure Vault Mid | B = Secure Vault High )
  - 2-4. Product Feature Codes
  - 5. Flash ( U = 1920k | T = 1152k )
  - 6. Temperature grade ( I = -40 to 125 °C )
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

# 8. Revision History

### Revision 1.2

March, 2026

- Updated ordering code EFR32FG25A021F256IM56-B to EFR32FG25A021F512IM56-B in Table 2.1. Ordering Information.
- Updated Table 4.57. Crypto Operation Timing for SE Manager API parameter description from ECC P-25519 timing to ECC Ed25519 timing.
- Updated Table 4.58. Crypto Operation Average Current for SE Manager API parameter description from ECC P-25519 timing to ECC Ed25519 timing.
- Updated Table 6.3. GPIO Alternate Function Table note for QFN56 / Standard Package OPN EFR32FG25A021F256IM56-B to EFR32FG25A021F512IM56-B.

### Revision 1.1

June, 2025

- Minor formatting and styling updates throughout document
- Updated wording in 3.7.4 Secure Debug with Lock/Unlock regarding availability of secure debug locking in both Secure Vault Mid and Secure Vault High devices.
- Updated Ordering Information
- Added $I_{LOAD}$ footnote to Table 4.3. DC-DC Converter
- Consolidate Spurious emissions specs in Table 4.17. 470 MHz Band +16 dBm RF Constant Envelope Transmitter Characteristics
- Added footnote on Capacitive Sense deprecation in Table 4.43. Analog Comparator (ACMP)
- Updated test conditions for Max spurious emissions in Table 4.24. 868 MHz Band RF Receiver Characteristics and in Table 4.25. 470 MHz Band RF Receiver Characteristics
- Updated Gecko Bootloader size in 4.21 Boot Timing
- Added footnote on bootloader size impacting boot timing in 4.21 Boot Timing

### Revision 1.0

January, 2023

- Entered min/max specs values for TBDs
- Added new specs for different testing conditions

### Revision 0.5

December, 2022

- Entered typical spec values for TBDs

### Revision 0.43

October, 2022

- Changed tests in 490 MHz Band RF SUN OFDM Transmitter Characteristics table
- Updated the detailed block diagram
- Updated Package Marking
- Changed test conditions
- Entered typical spec values for TBDs
- Removed Thermistor Driver Spec Table
- Added typical performance curves

### Revision 0.42

October, 2022

- Entered typical spec values for TBDs

**Revision 0.41**

September, 2022

- Entered typical spec values for TBDs
- Removed some tests
- Removed O-QPSK tables

**Revision 0.4**

September, 2022

- Added OPN Decoder
- Changed test conditions
- Entered typical spec values for TBDs
- Renamed test symbol
- Added matching network for 470 MHz

**Revision 0.3**

June, 2022

- Clarify test conditions
- Update tested parameters
- Include Crypto Operation Characterization

**Revision 0.2**

January, 2022

- Changed Test Conditions and footnotes for several specifications to correct errors and clarify
- Changed Operating Conditions to be more clear
- Updated some security system details
- Changed Typical Connection Diagrams and matching network
- Corrected errors

**Revision 0.1**

July, 2021

Initial release.

SILICON LABS
CONNECTED INTELLIGENCE

# The Leading Innovator in Low-Power Wireless.

**IoT Portfolio**
silabs.com/products

**Simplicity Studio**
silabs.com/simplicity

**Quality**
silabs.com/quality

**Support & Community**
silabs.com/community

---



---


SILICON LABS CONNECTED INTELLIGENCE

400 West Cesar Chavez
Austin, TX 78701 | USA

www.silabs.com